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# MS-7175 Version: 3.0

Intel (R) Grantsdale (GMCH) + ICH6 Chipset  
Intel Tejas & Prescott LGA775 Processor

## CPU:

**Intel Tejas/Prescott - 3.6G**

## System Chipset:

**Intel Grantsdale - GMCH (North Bridge)**

**Intel ICH6 (South Bridge)**

## On Board Chipset:

**AC97 Codec -- ALC880**

**LPC Super I/O -- Winbond 83627THF**

**LAN-- Intel - 10/100 PHY 82562EZ**

**Intel - GIGA (PCI) 82541PI**

**CLOCK Gen-- ICS954119**

**IEEE 1394 -- VIA VT6307**

**H/W Monitor -- W83792AD**

**BIOS -- FWH FLASH 4M**

## Main Memory:

**Dual Channel DDR 2 \* 4 (Maximum to 4GB)**

## Expansion Slots:

**PCI Express X16 SLOT \* 1**


**PCI 1.2.3 SLOT \* 3**

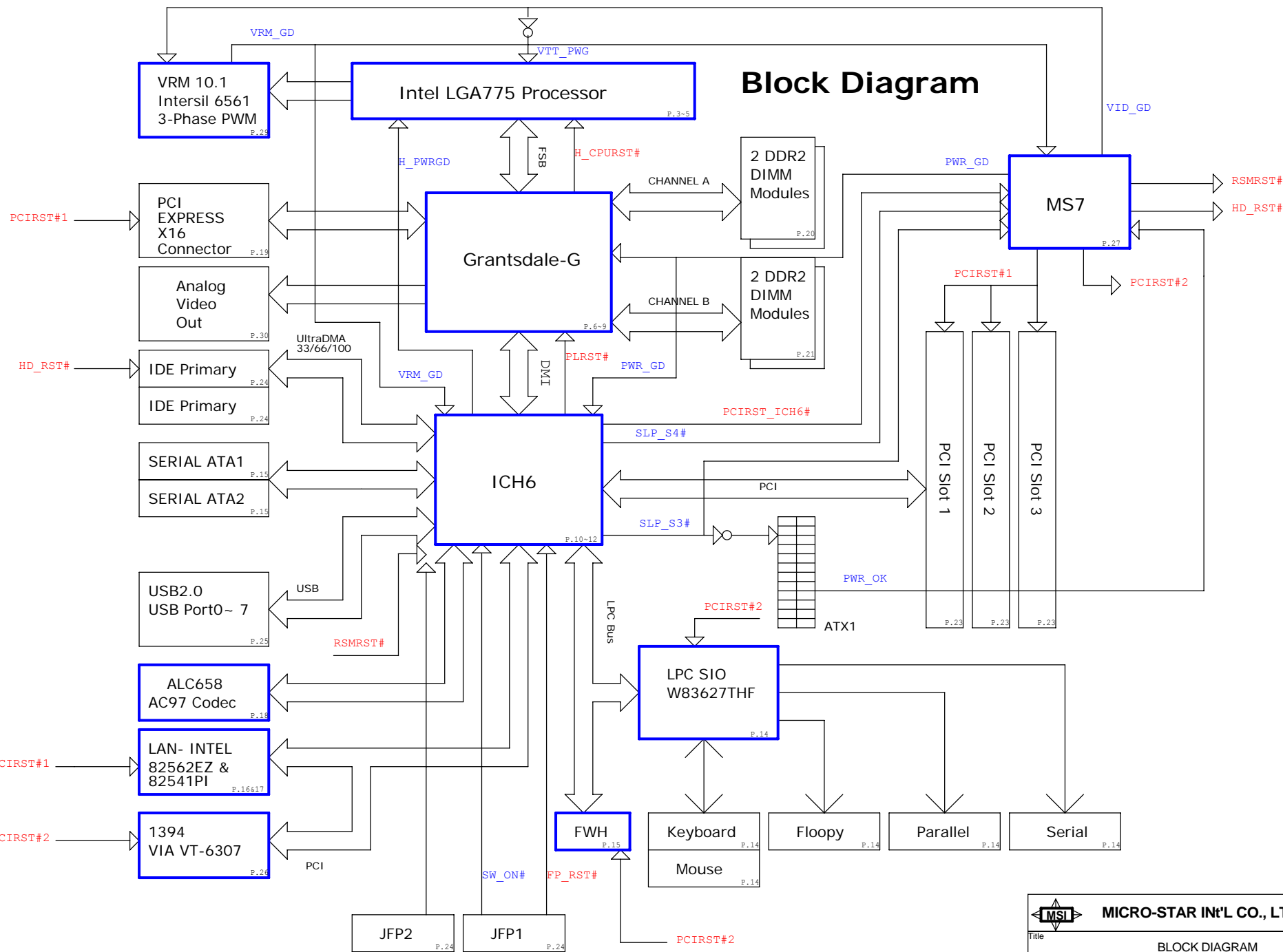
## Intersil PWM:

**Controller: HIP6565ACV**

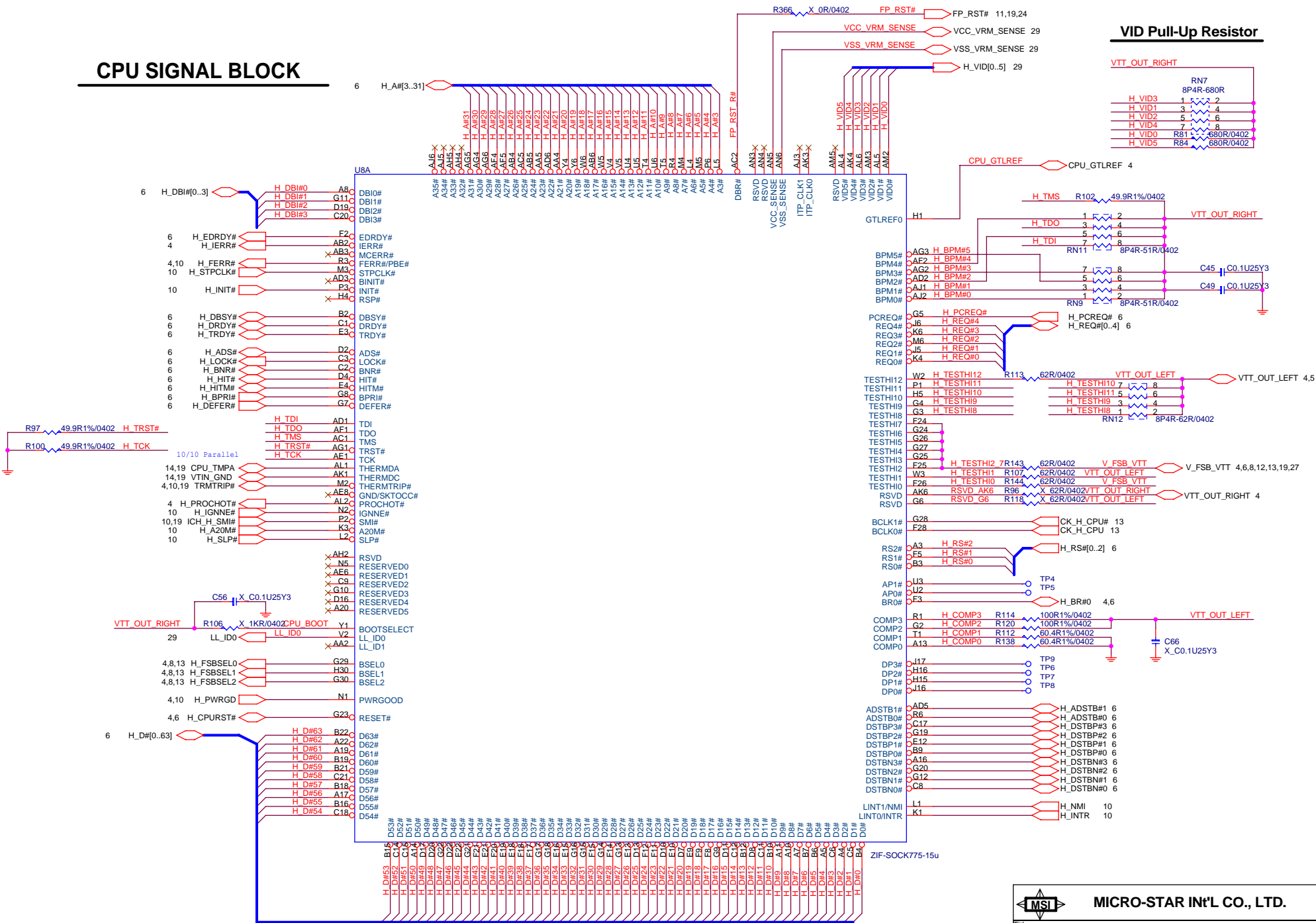
**Driver: HIP6614ACB + HIP6612ACB**

MSI Model Name	OPT	Description
MS-7175 (601-7175-01S)	L	915G+10/100Lan
MS-7175 (601-7175-02S)	GL	915G+GigaLan
MS-7175 (601-7175-03S)	GF	915G+GigaLan +ASF2.0

		MICRO-STAR INT'L CO., LTD.	
Title		COVER SHEET	
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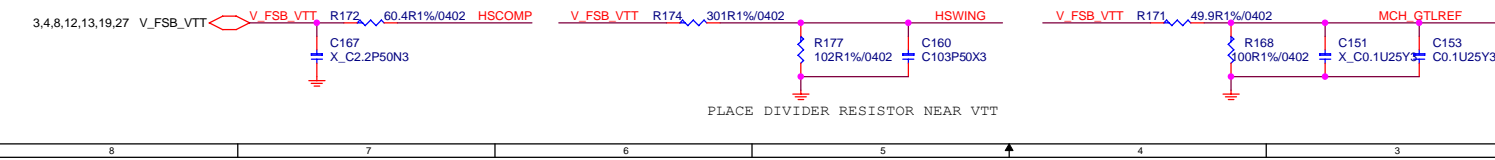
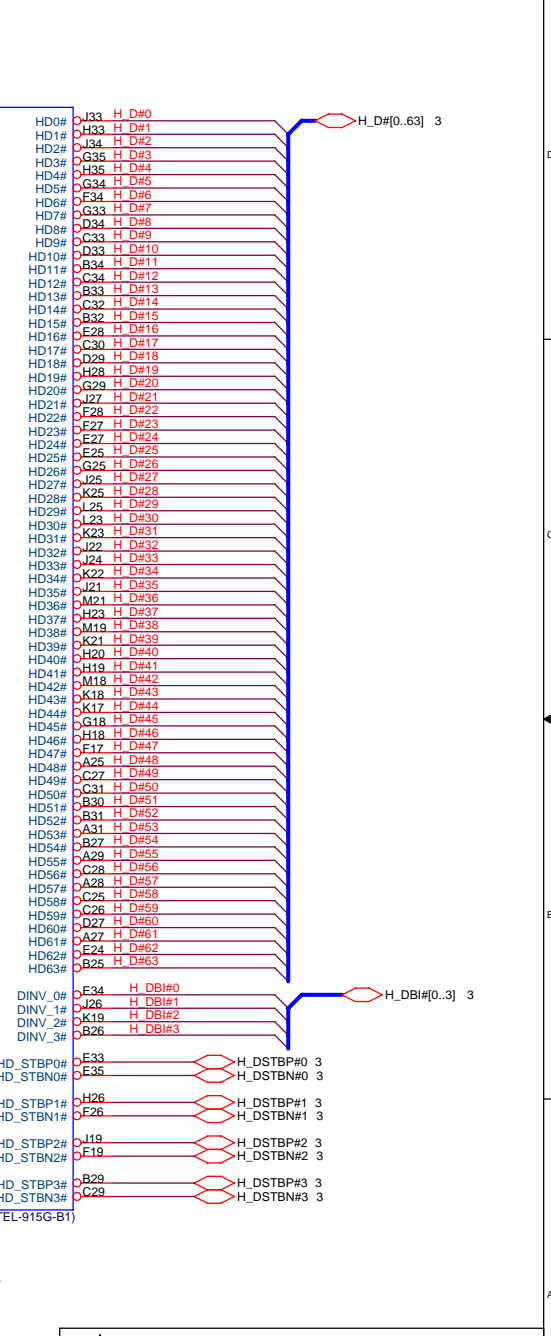
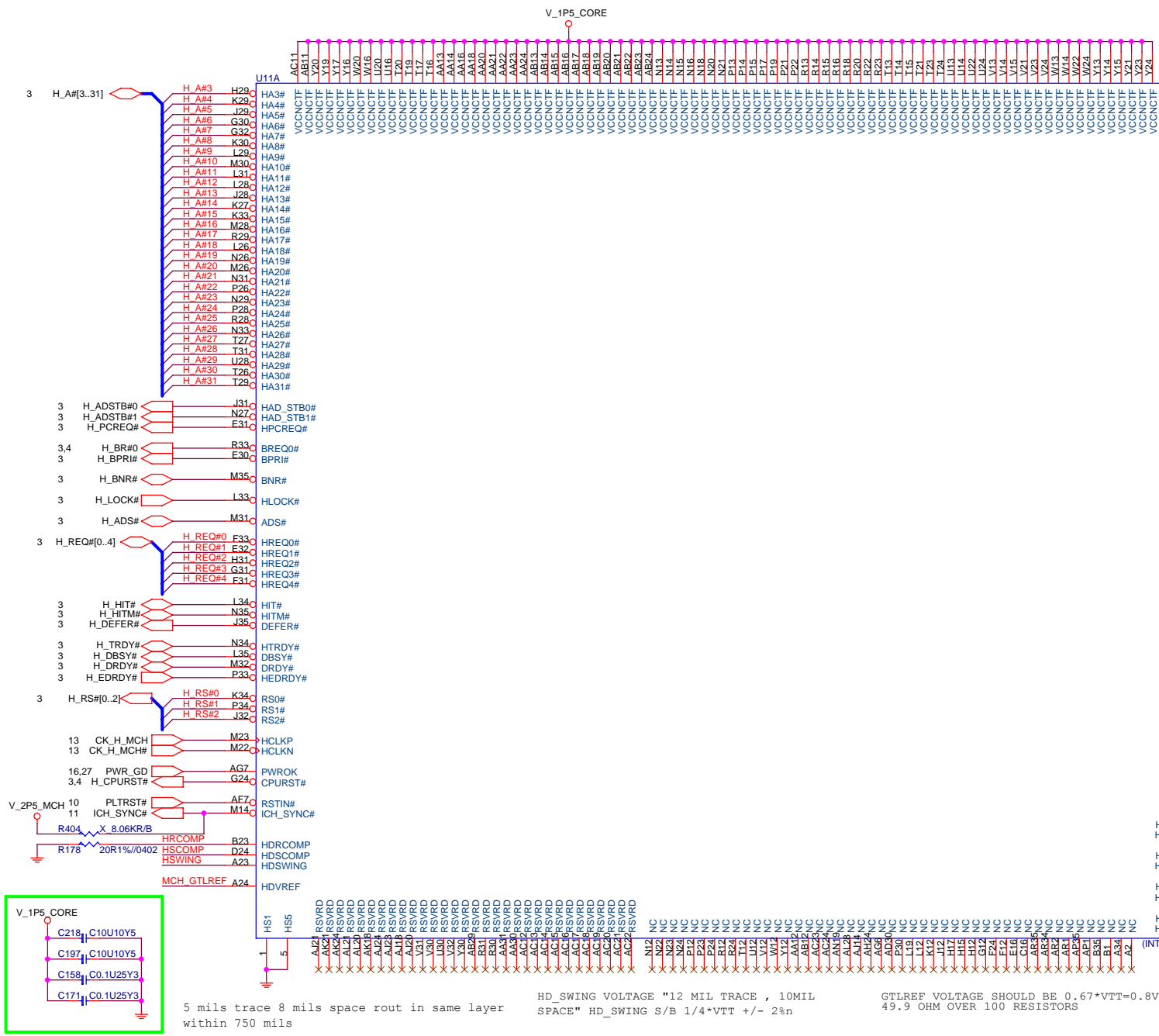



# CPU SIGNAL BLOCK







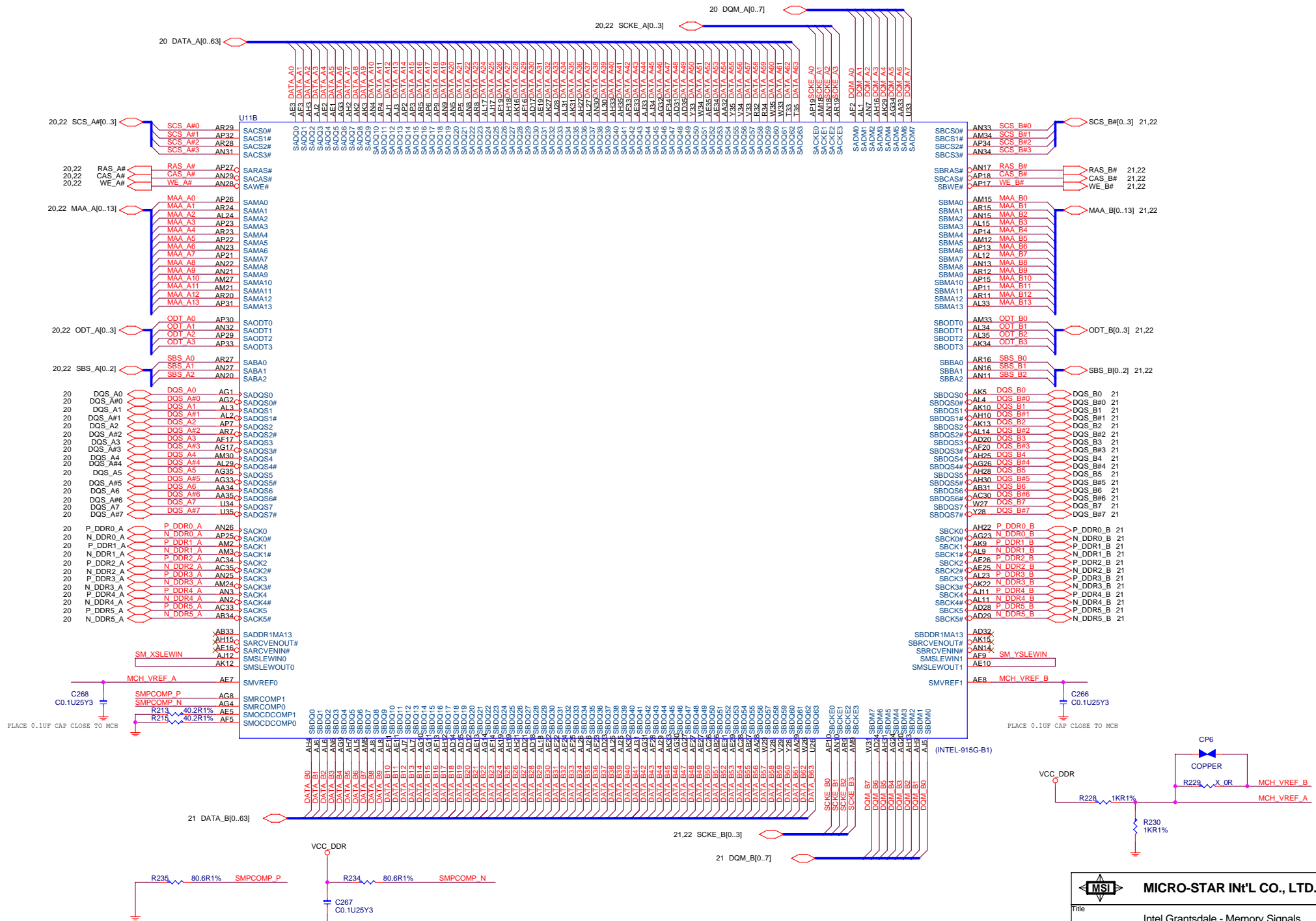


**MICRO-STAR IN'L CO., LTD.**

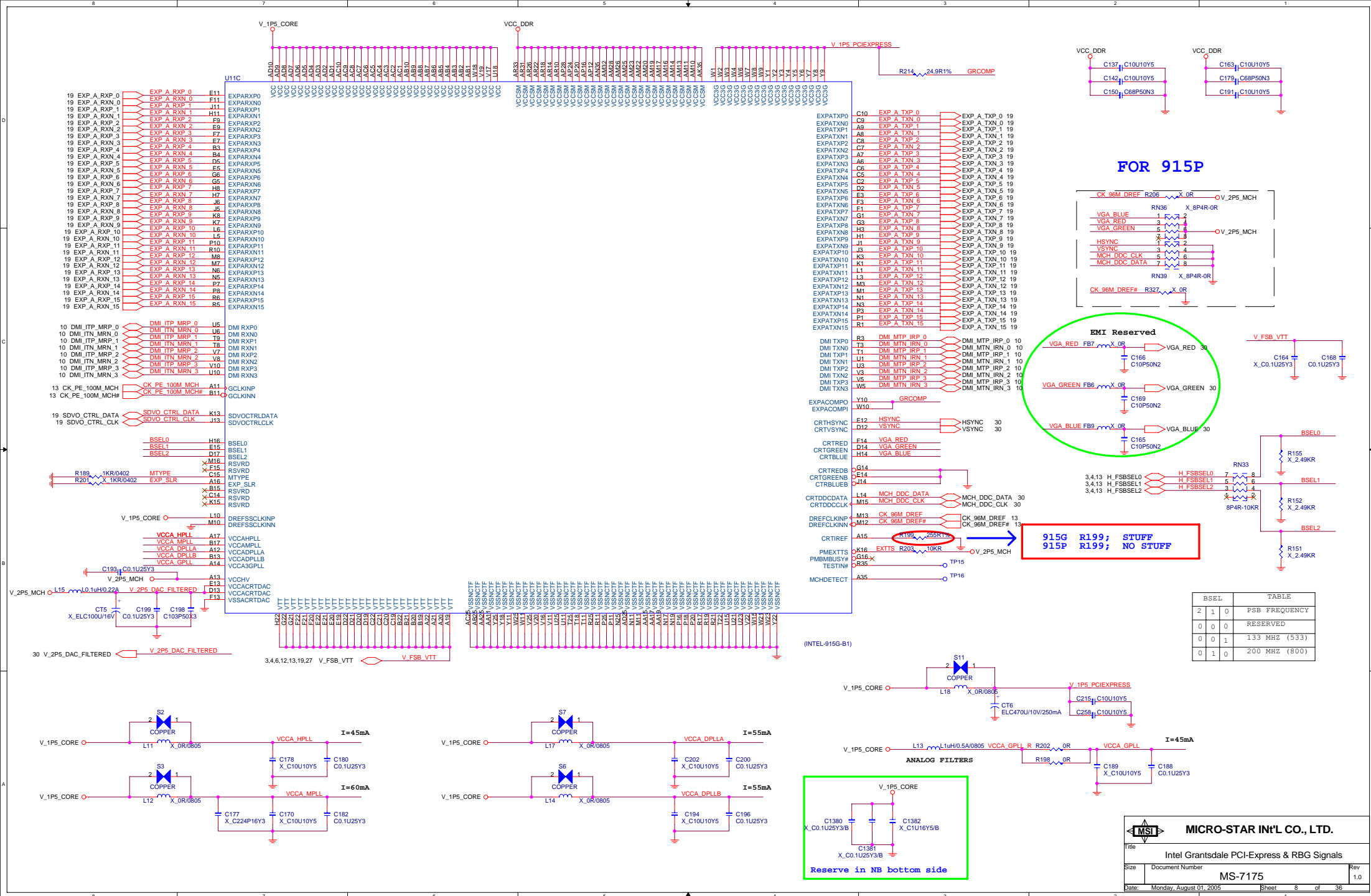
TitleIntel Grantsdale - CPU Signals

Size	Document Number	Rev
	MS-7175	1.0

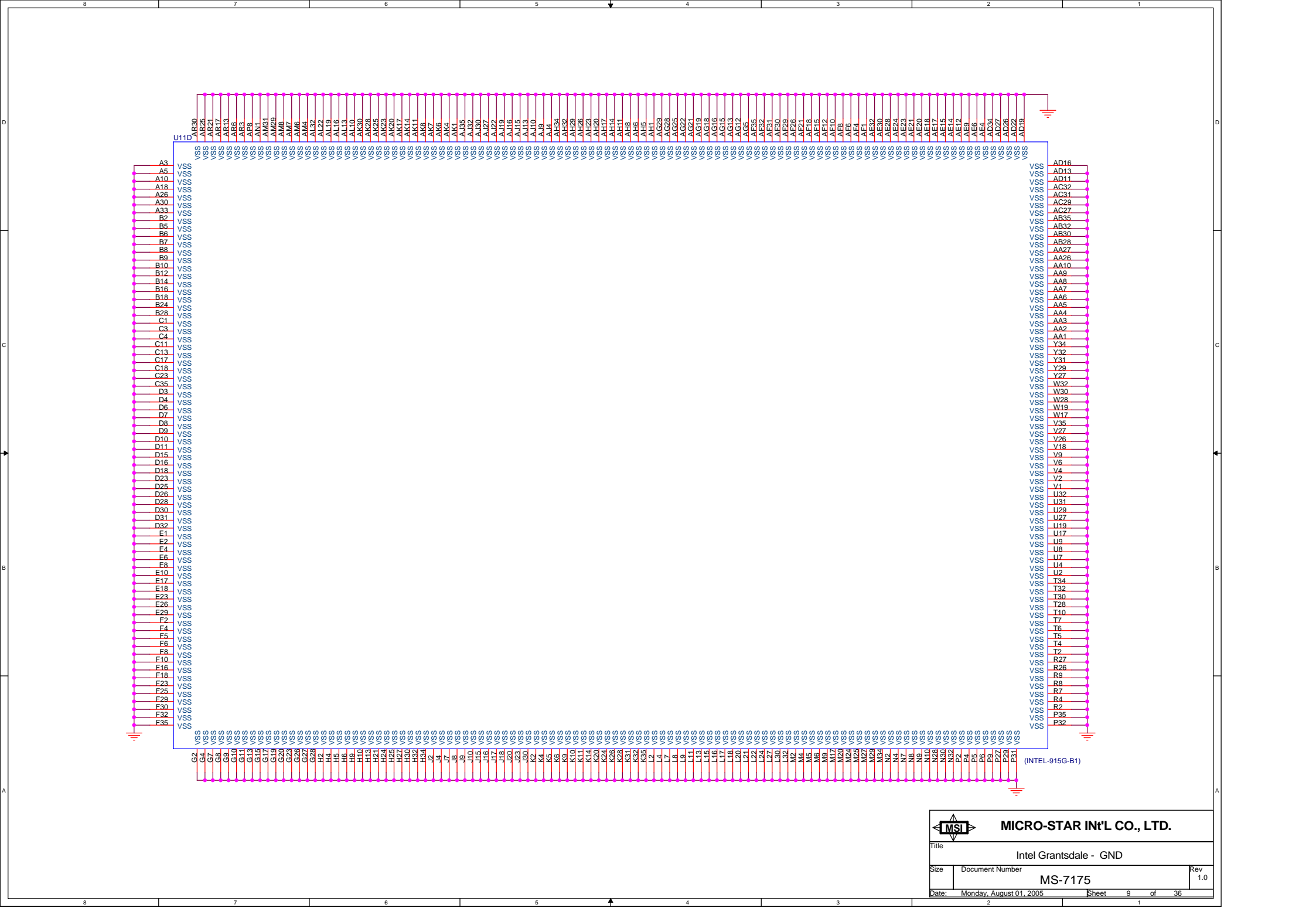
Date: Monday, August 01, 2005	Sheet 6 of 36
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**MICRO-STAR INT'L CO., LTD.**

Title

Intel Grantsdale - GND

Size

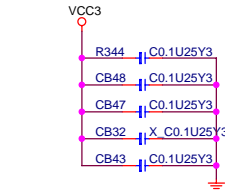
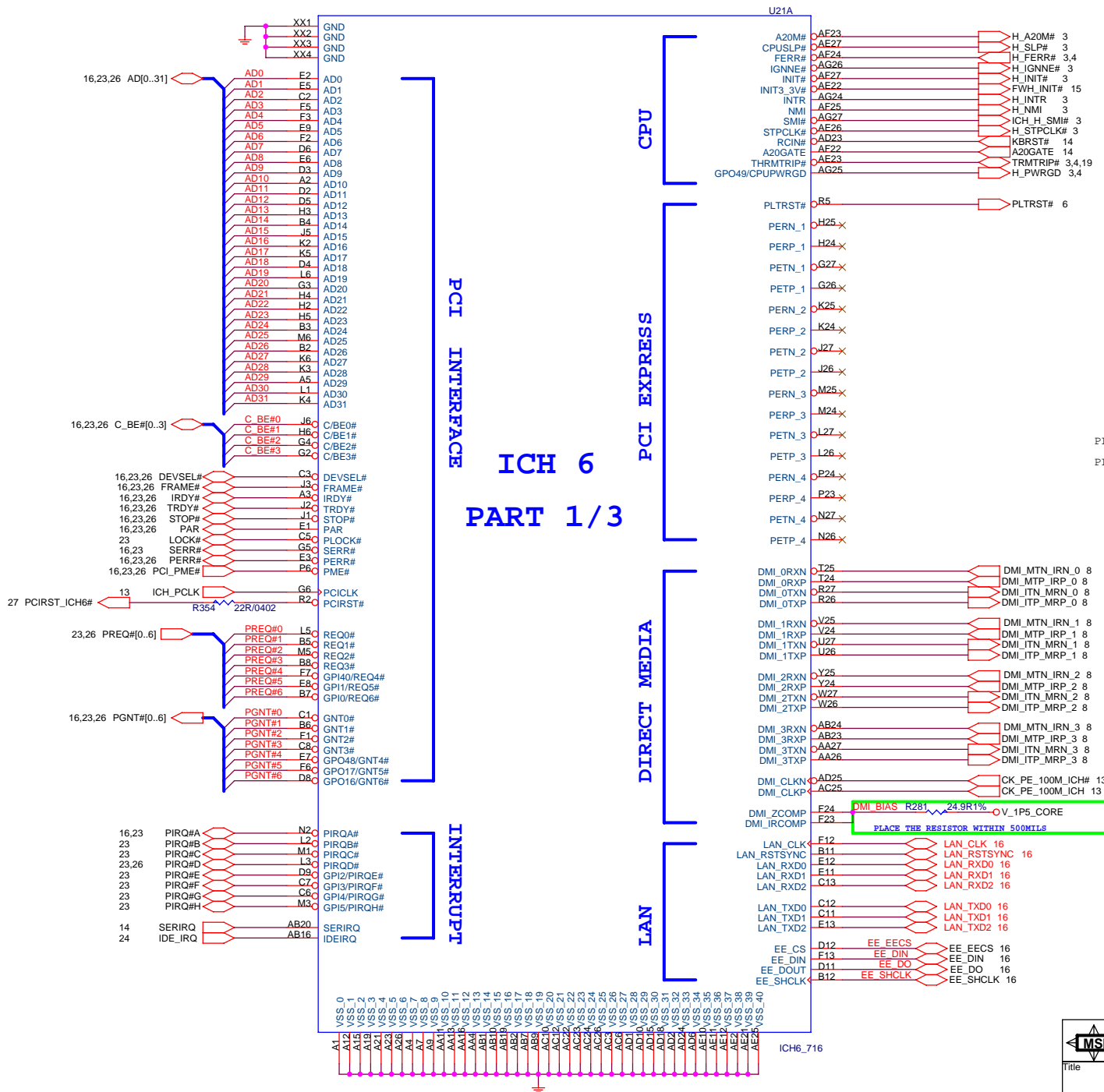
Document Number

Rev  
1.0

Date: Monday, August 01, 2005

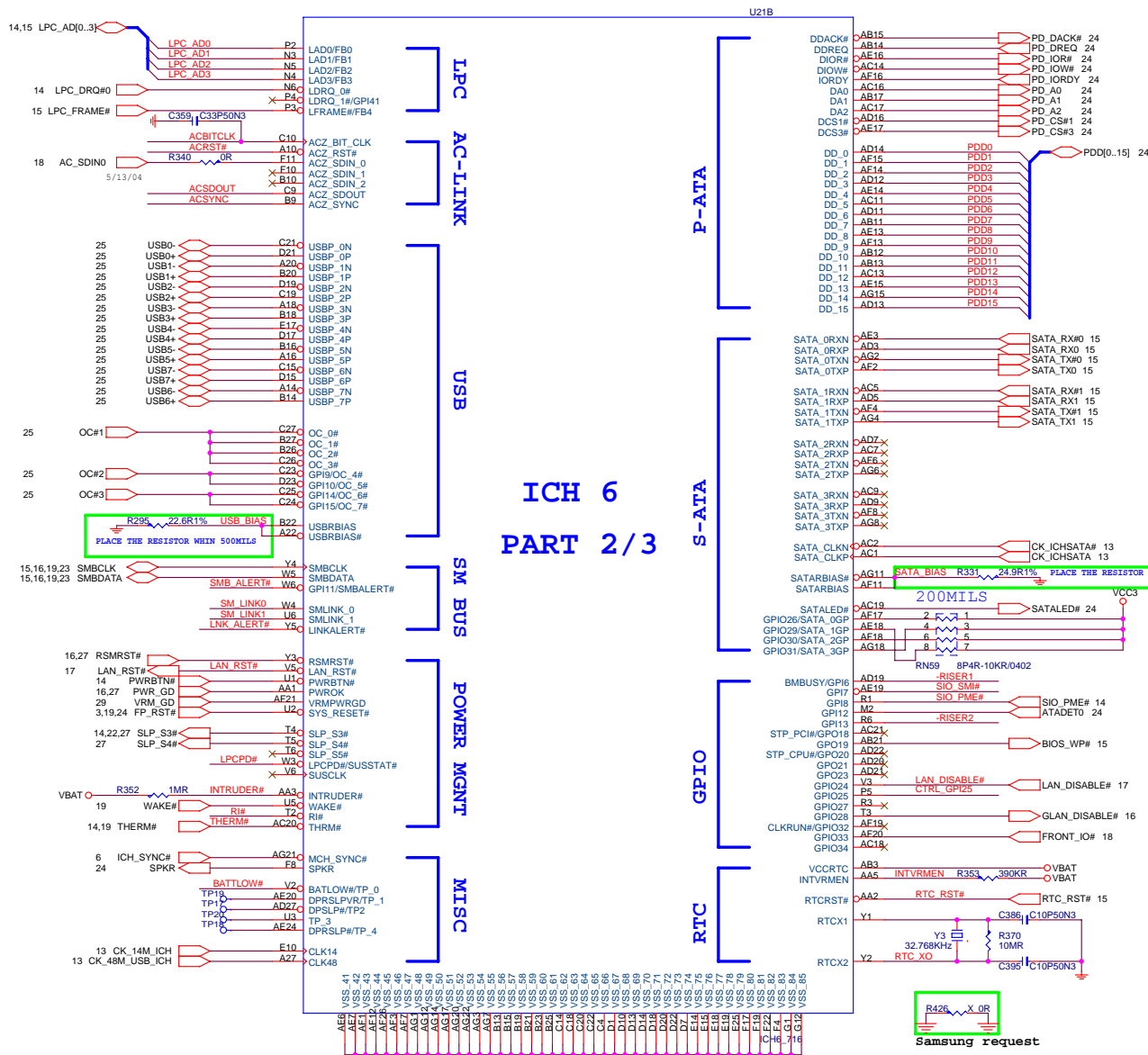
Sheet 9 of 36

MS-7175



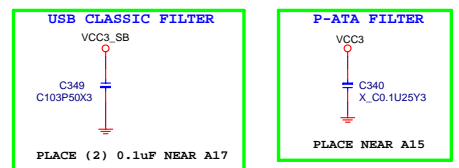
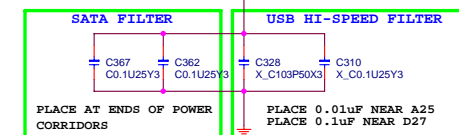
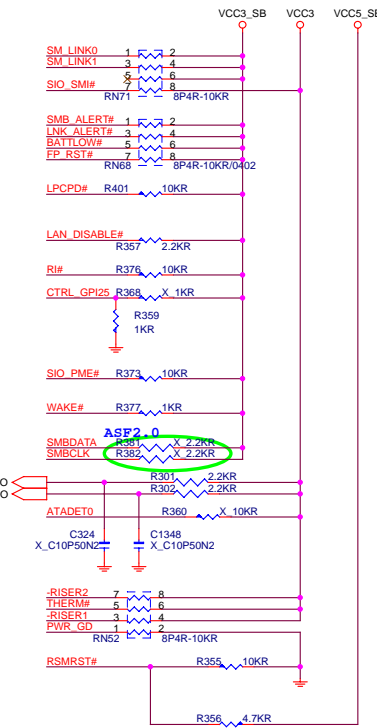
PLACE 1 EACH NEAR A3 & F1  
PLACE REMAINDER ANUWHERE



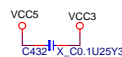


## ICH6 STRAPPING RESISTORS

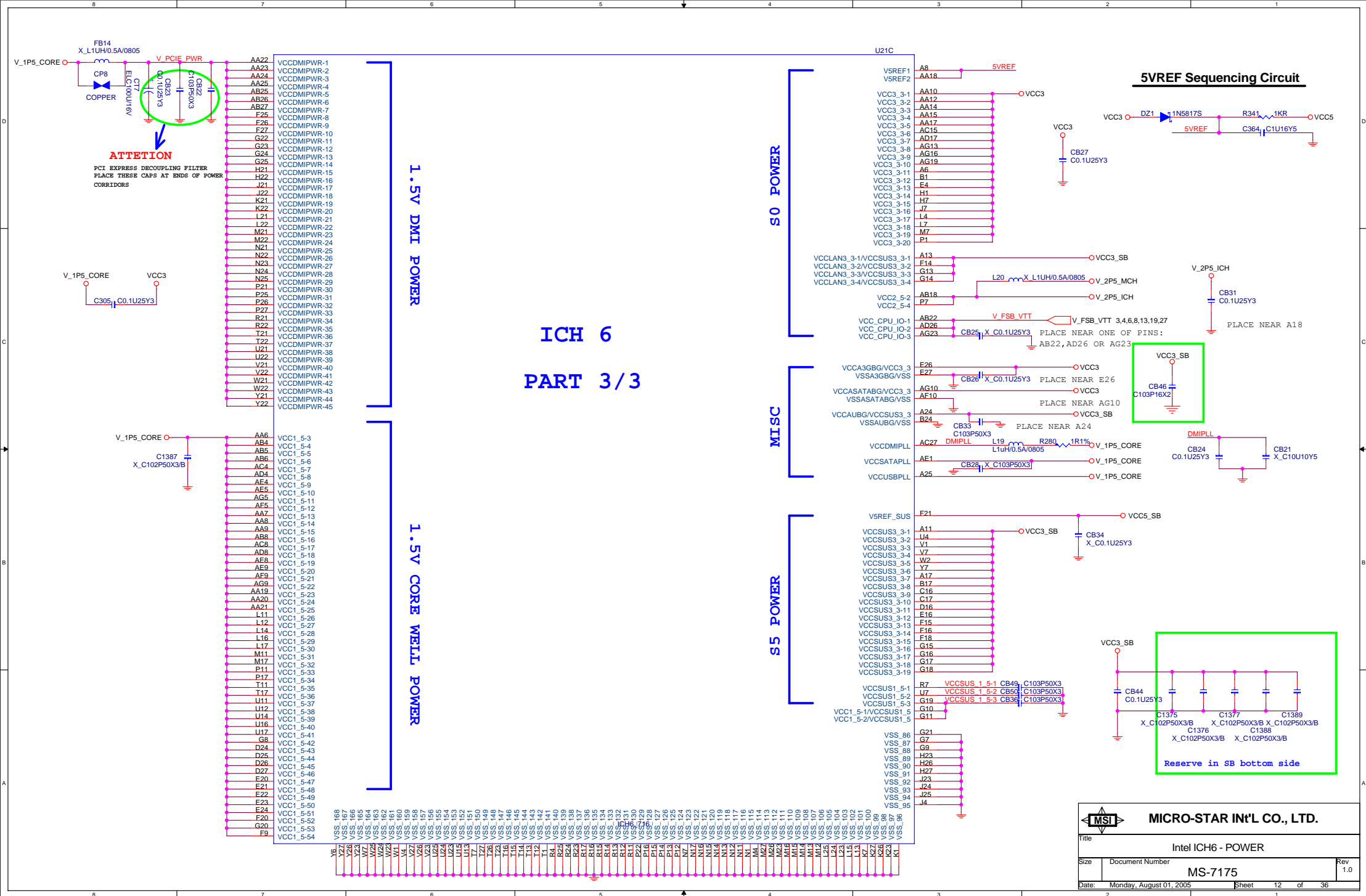
ALL COMPONENTS CLOSE TO ICH6  
Trace length is less than 3inchs to ICH6.



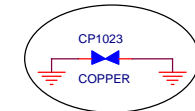
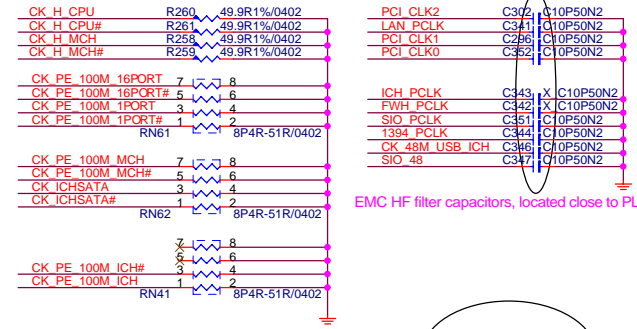
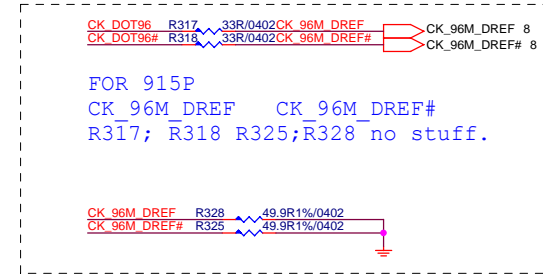
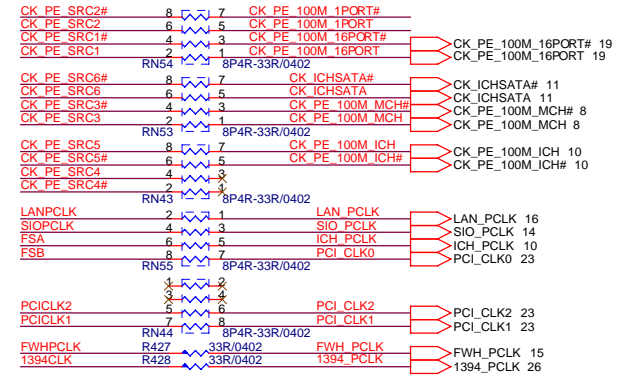
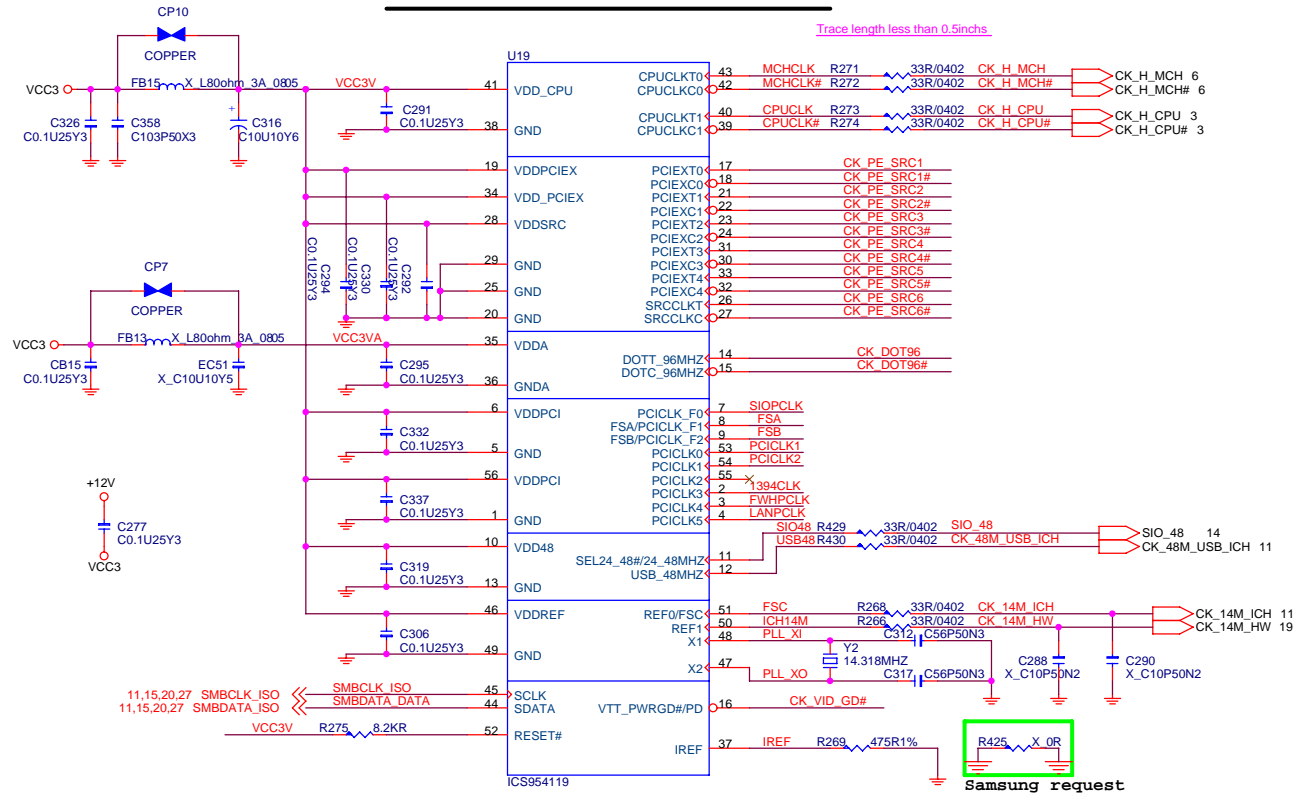
EMI Solution



MSI MICRO-STAR INT'L CO., LTD.	
Title Intel ICH6 - LPC & ATA & USB & GPIO	
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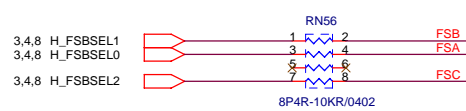


## Clock Generator - ICS954119

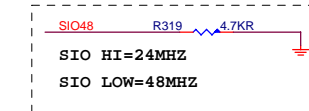
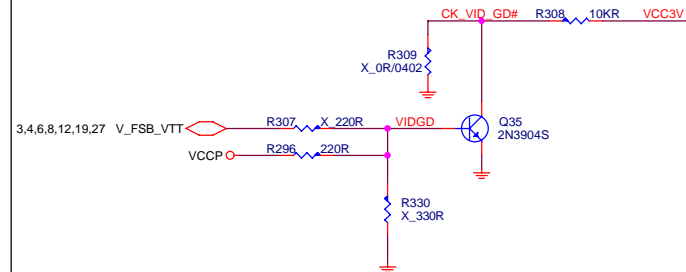


### BSEL[0..2] Level Shift

	H_FSB_SEL		
CPU	0	1	2
133MHz	1	0	0
200MHz	0	1	0



### Clock Generator VTT Power Down Block



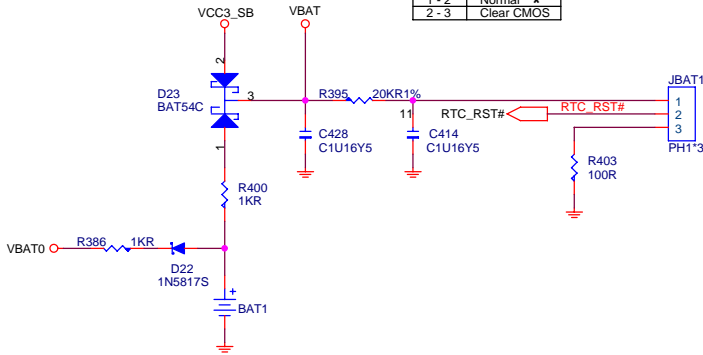




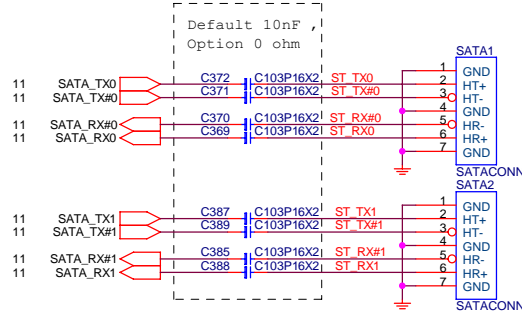
## RTC BLOCK

Close to Pin AA2 of ICH6.

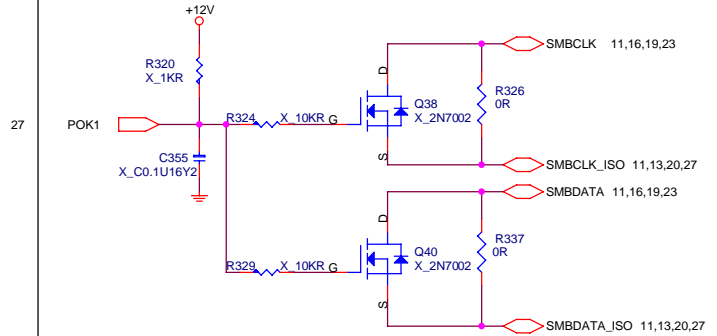
CLEAR CMOS		
1-2	Normal	★
2-3	Clear CMOS	



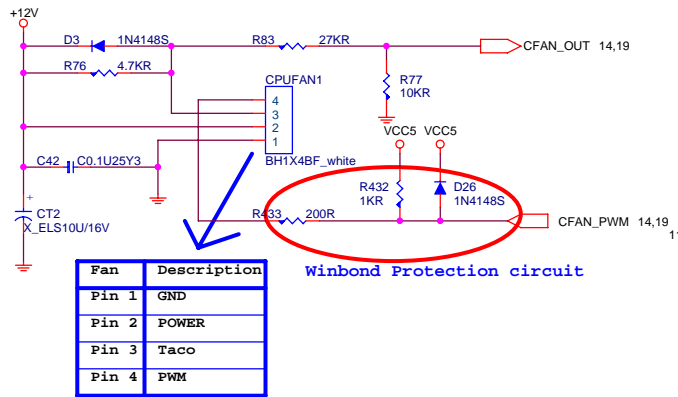
## SATA CONNECTOR BLOCK



## SMBUS ISOLATE

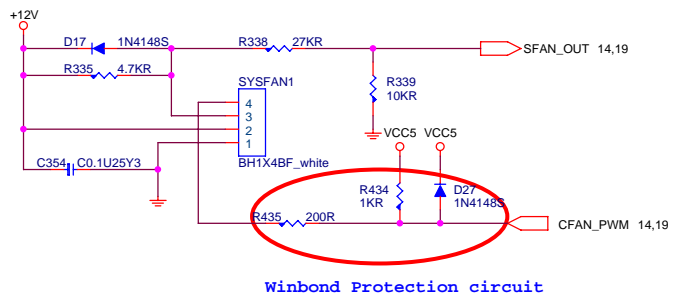


## CPU FAN



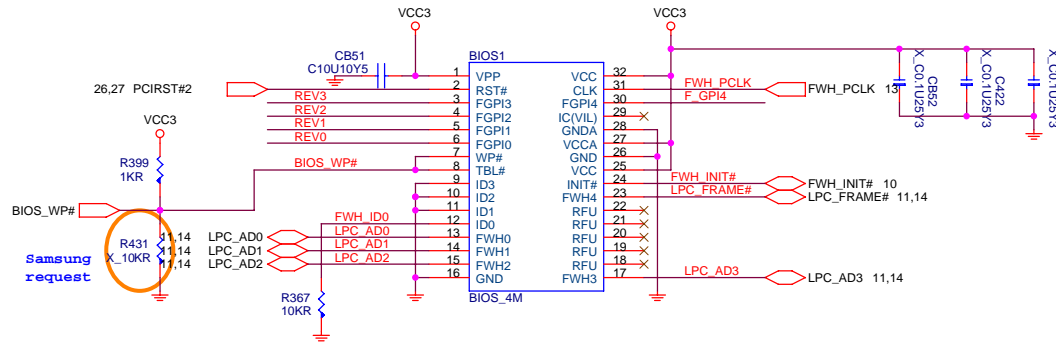
Winbond Protection circuit

## SYSTEM FAN



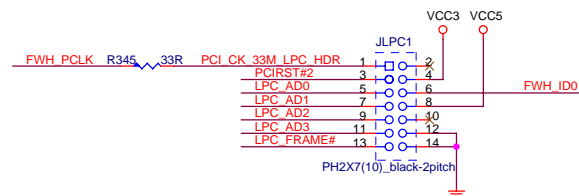
Winbond Protection circuit

## FIRMWARE HUB (FWH)

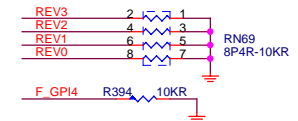


## LPC Debug Port

If you place the jumper very closed to FWH bios socket, please use the same clock with FWH. But if you can not place it so close, please use another clock to support it.



## FWH RESISTORS





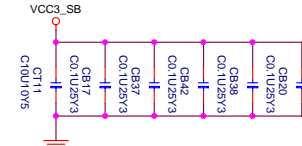
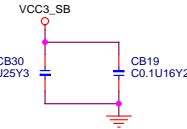
10/100: Intel 82562EZ -- B06-562EZ05-I06  
Giga: Intel 82541PI -- B06-541PI05-I06

### FOR 82562EZ

### FOR 82541PI

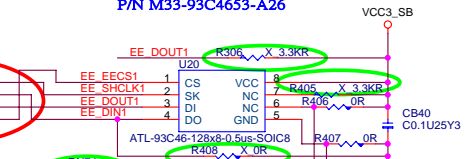
1.8V RAIL ONLY REQUIRED WITH  
82541GI CONTROLLER. NOT  
CONNECTED WITH 82562EZ

FOR 82562EZ  
1.2V RAIL ONLY REQUIRED WITH  
82541GI CONTROLLER

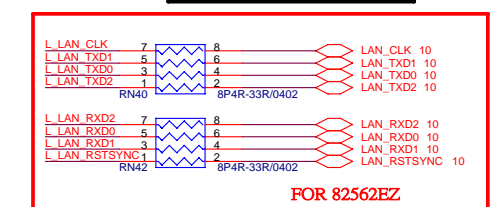


82541PI/82562EZ VCC3.3V Decoupling CAPS

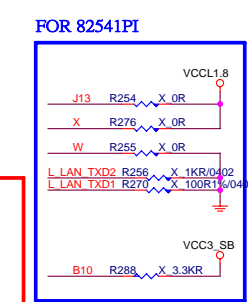
Support ASF2.0 mode: eeprom P/N  
M33-2516013-A26  
Non support ASF2.0 mode: eeprom  
P/N M33-93C4653-A26



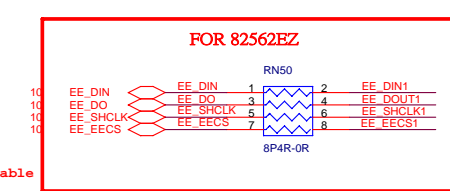
Support ASF2.0:  
Stuff RN74, R306, R405, R408



FOR 82562EZ



FOR 82541PI



FOR 82562EZ

TCK = "1" to Disable  
82562EZ LAN

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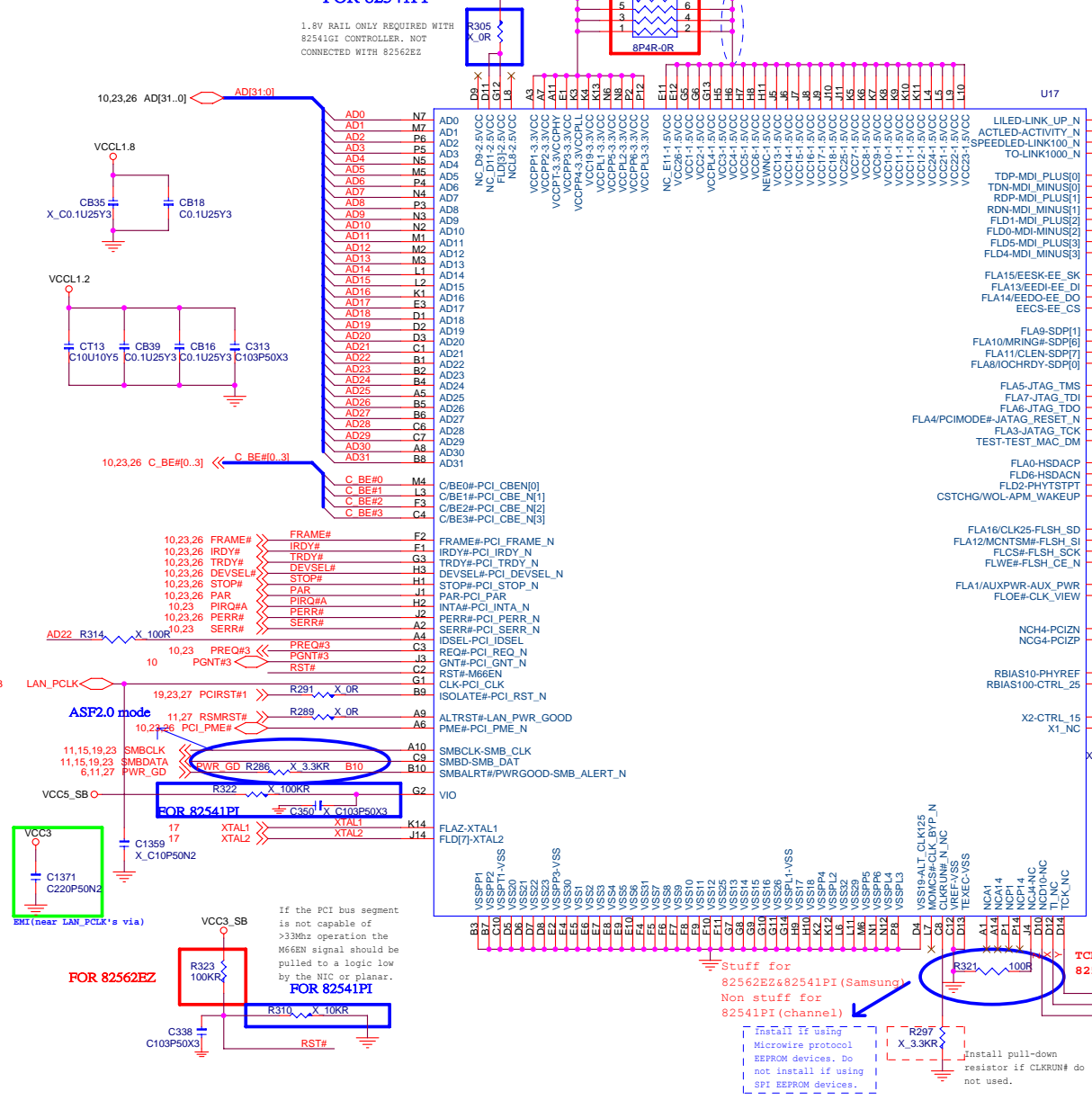
LAN Intel 82562EZ/82541PI

MS-7175

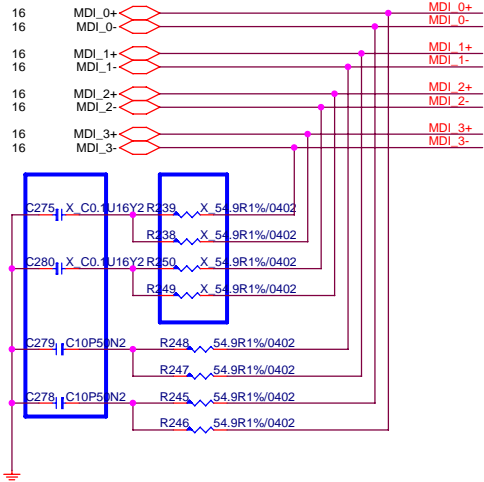
Rev 1.0

Monday, August 01, 2005

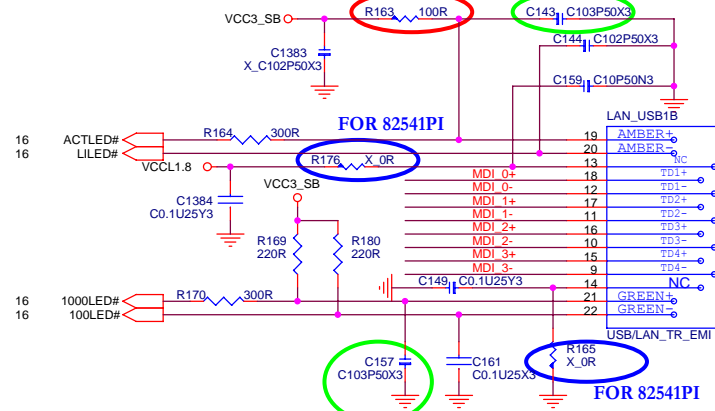
Sheet 16 of 36



FOR 82541PI

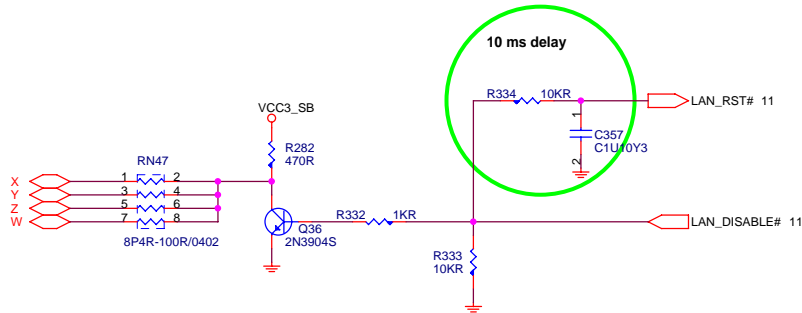


FOR 82562EZ



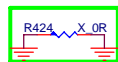
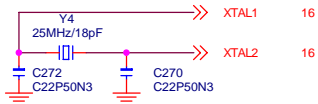
10/100:N58-22F0061-F02  
 Giga: N58-22F0081-S42

10 ms delay

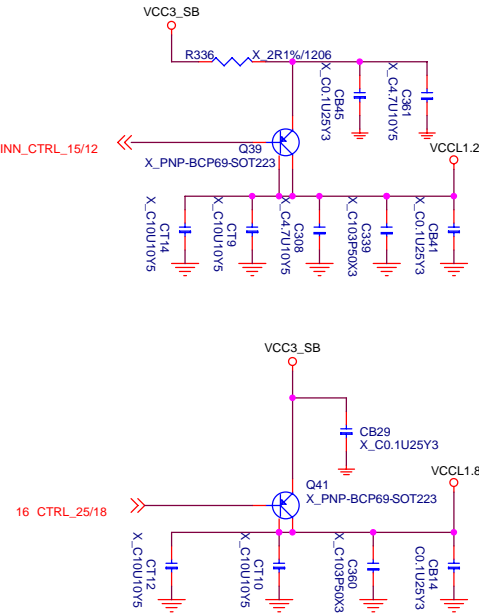


### LAN Crystal

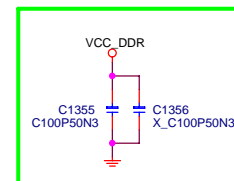
THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.



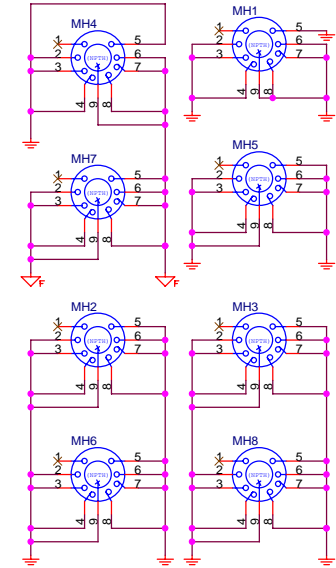
Samsung request



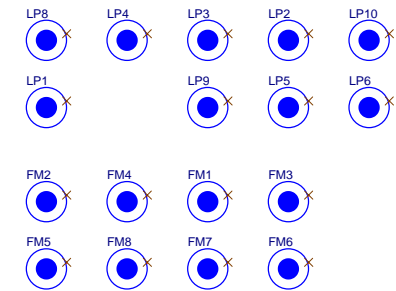
EMI Suggestion:Near MH5



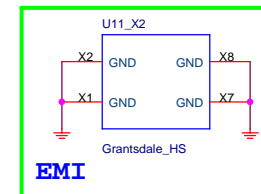
### Mounting Holes



### Optics Orientation Holes



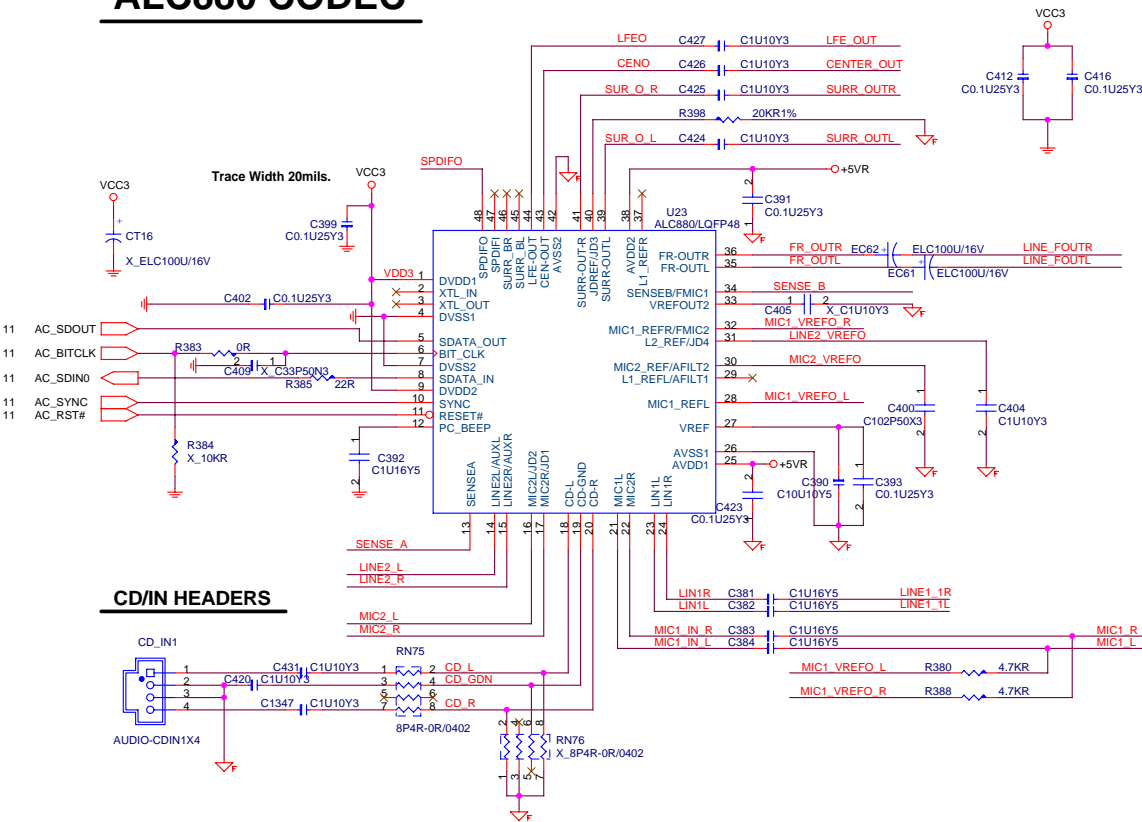
### Simulation



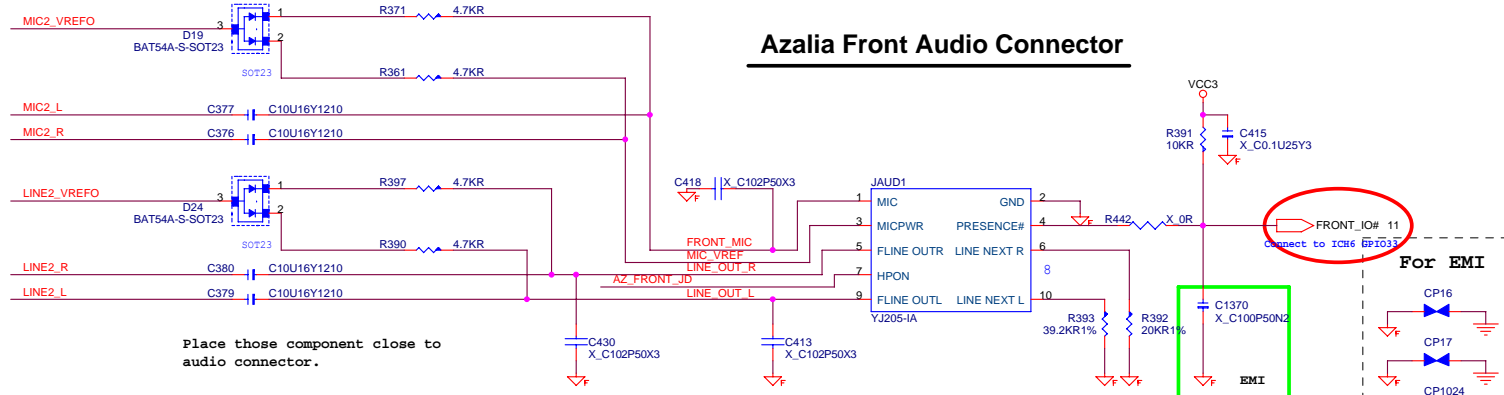
MICRO-STAR INT'L CO., LTD.

Title			LAN Connector
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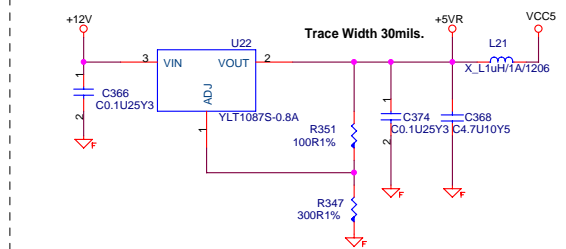
# ALC880 CODEC



## Azalia Front Audio Connector

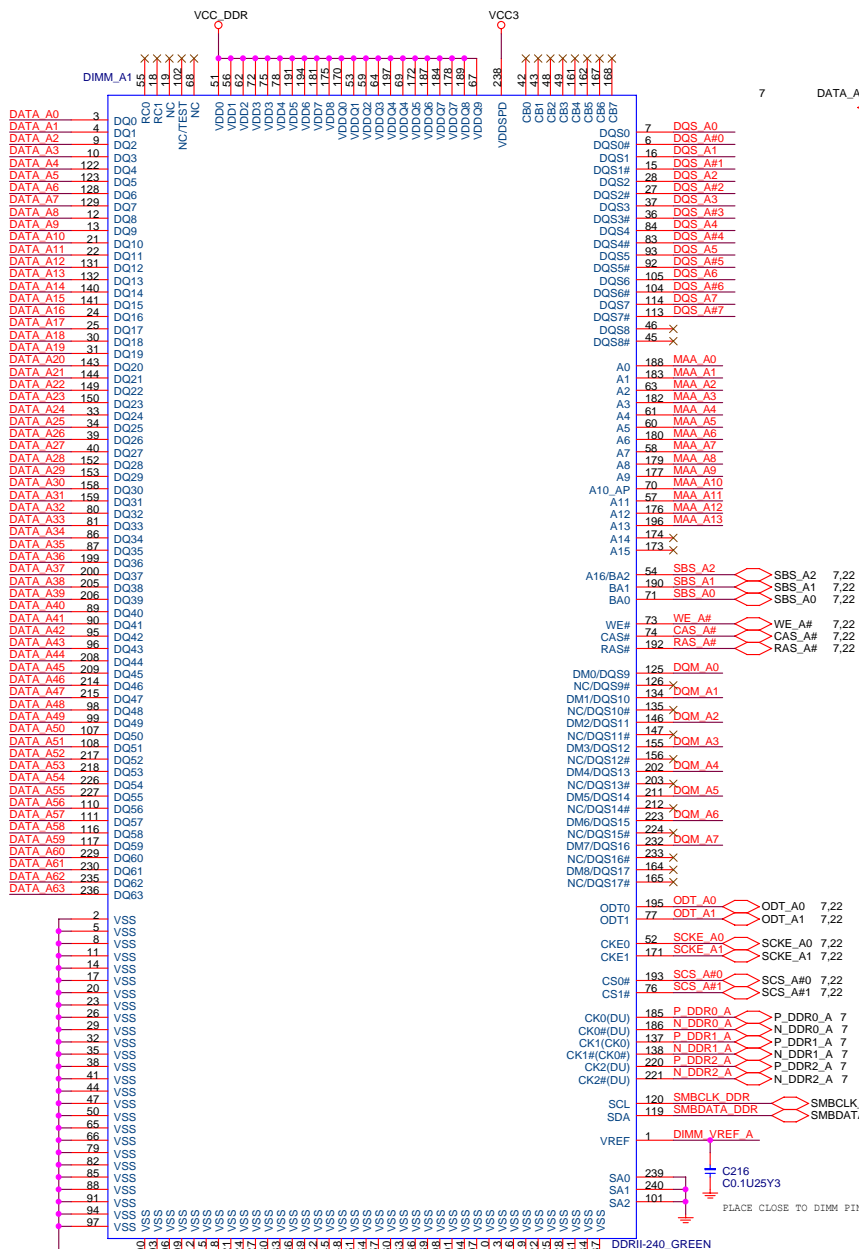


## AUDIO CODE REGULATORS

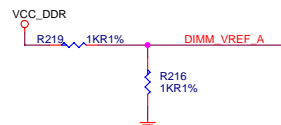


MSI MICRO-STAR INT'L CO., LTD.			
Title			
Azalia Codec(ALC880)			
Size	Document Number	Rev	
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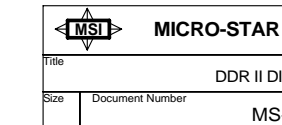
DDR2 DIMM\_A1



ADDRESS: 000  
0xA0



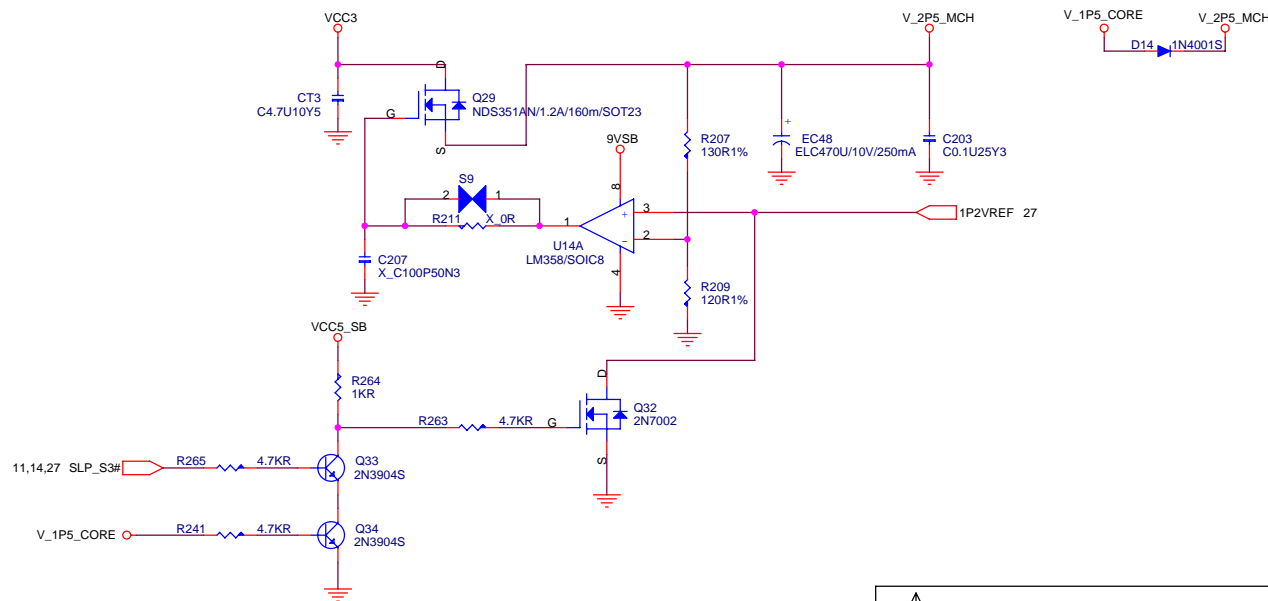
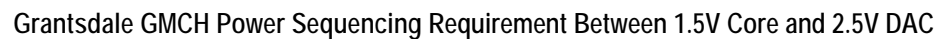
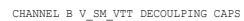
DDR2 DIMM\_A2



ADDRESS: 001  
0xA2

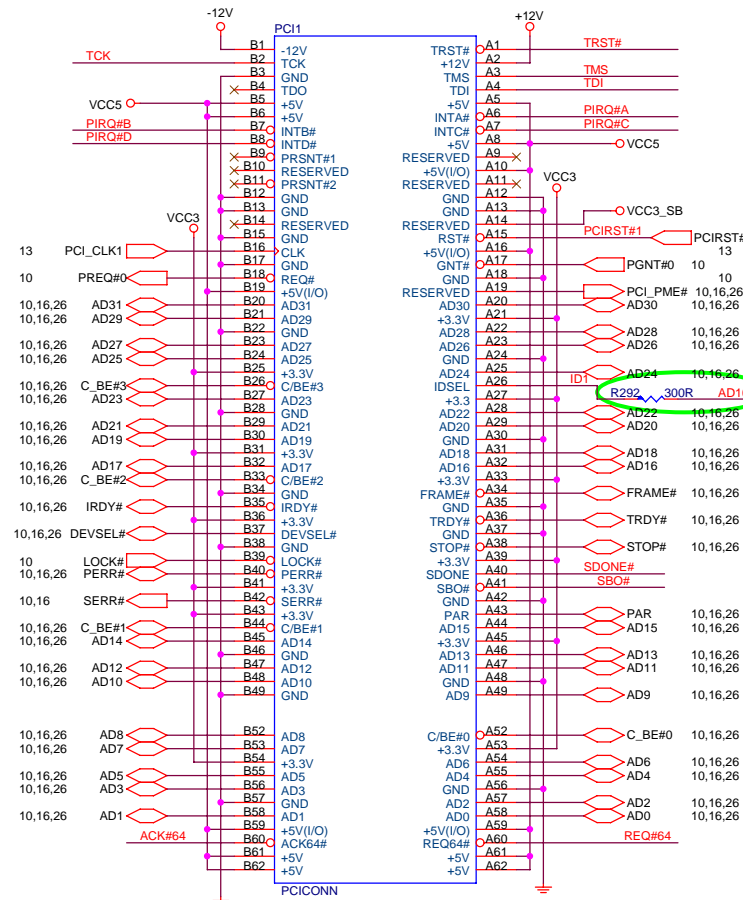






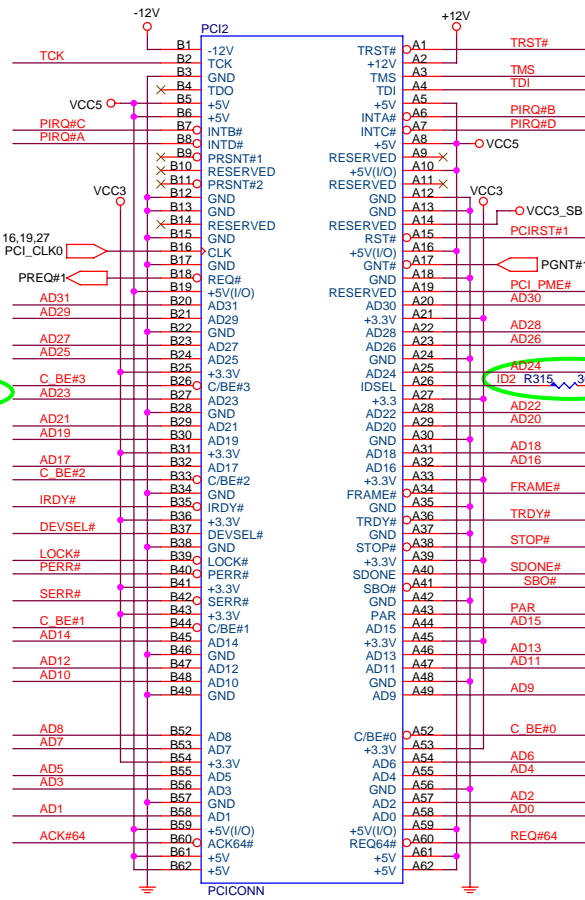


# PCI SLOT 1 (PCI VER: 2.2 COMPLY)



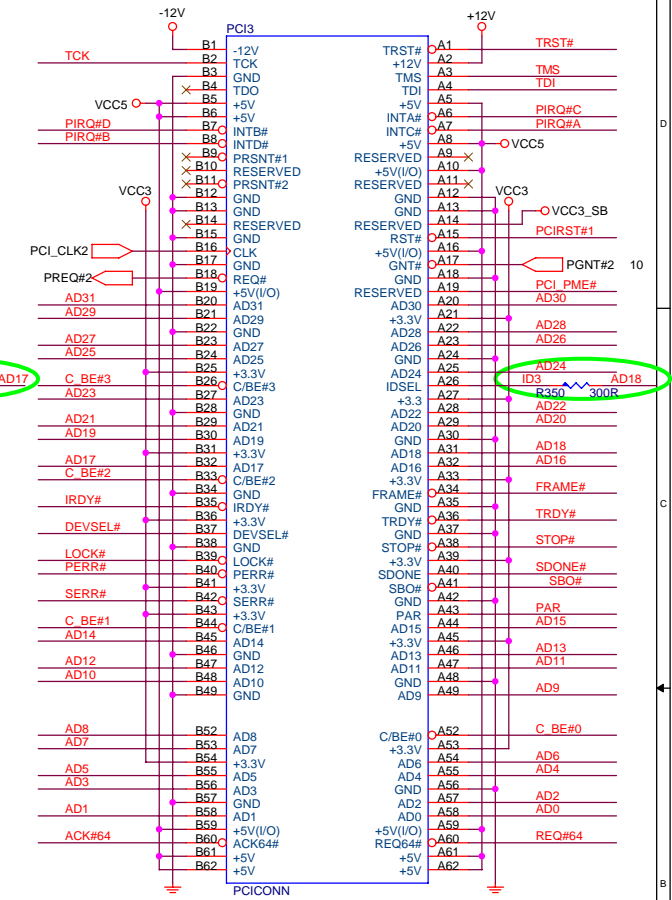
IDSEL = AD16  
MASTER = PREQ#0  
PIRQ#A

# PCI SLOT 2 (PCI VER: 2.2 COMPLY)



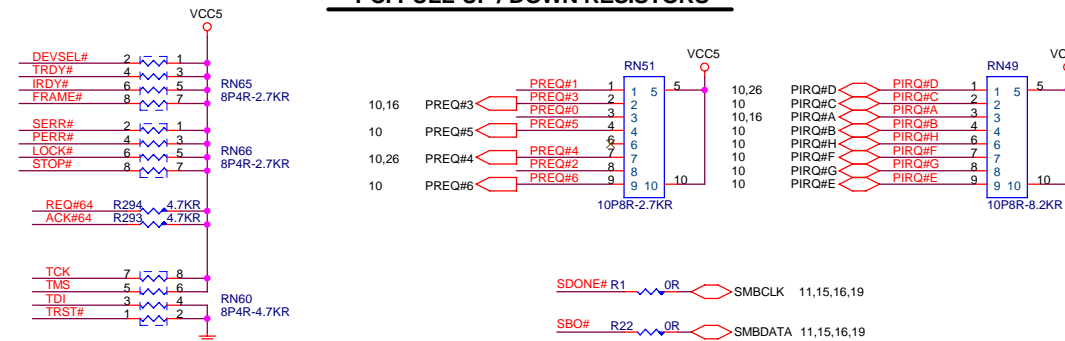
IDSEL = AD17  
MASTER = PREQ#1  
PIRQ#B

# PCI SLOT 3 (PCI VER: 2.2 COMPLY)

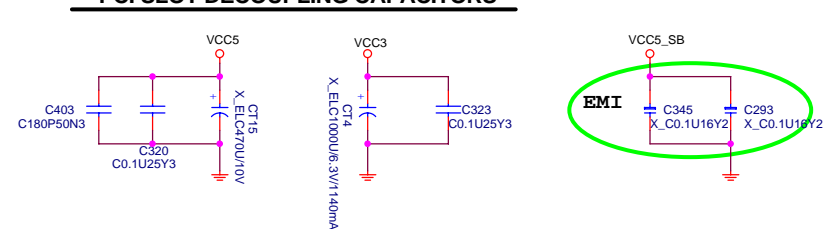


IDSEL = AD18  
MASTER = PREQ#2  
PIRQ#C

## PCI PULL-UP / DOWN RESISTORS

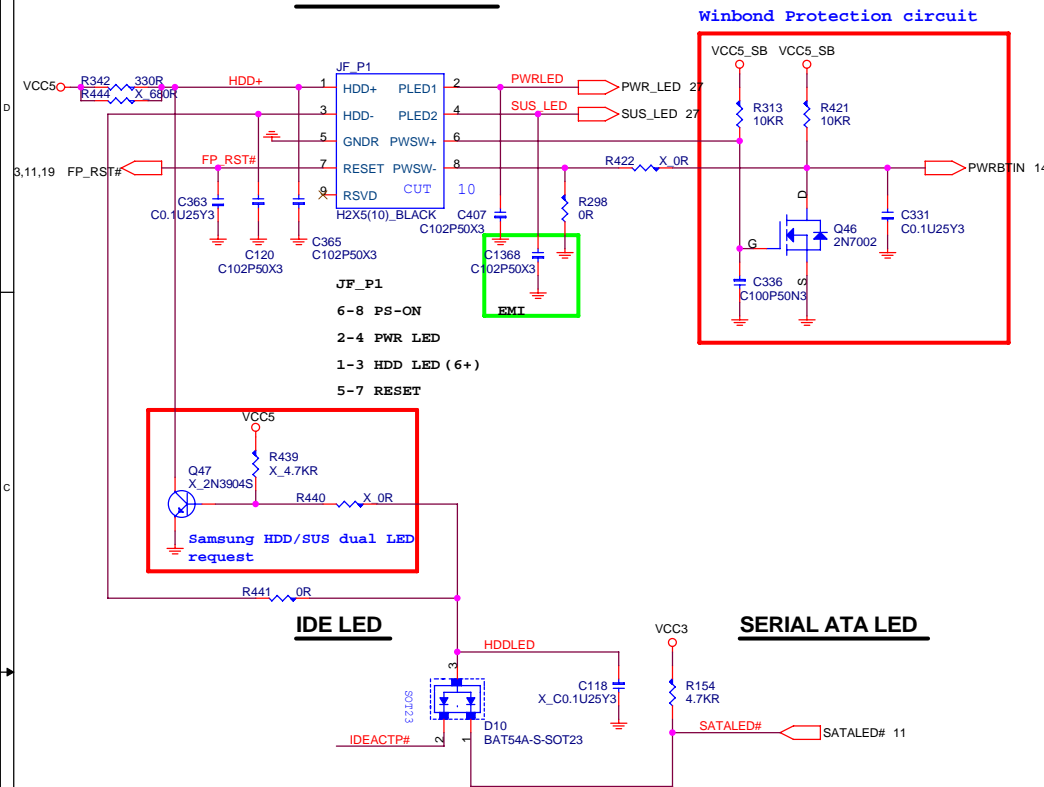


## PCI SLOT DECOUPLING CAPACITORS

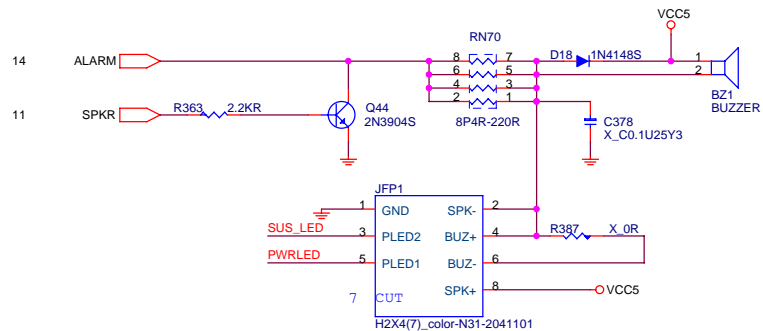


		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title			
PCI 1 & 2 & 3 Slots			
Size	Document Number	Rev	
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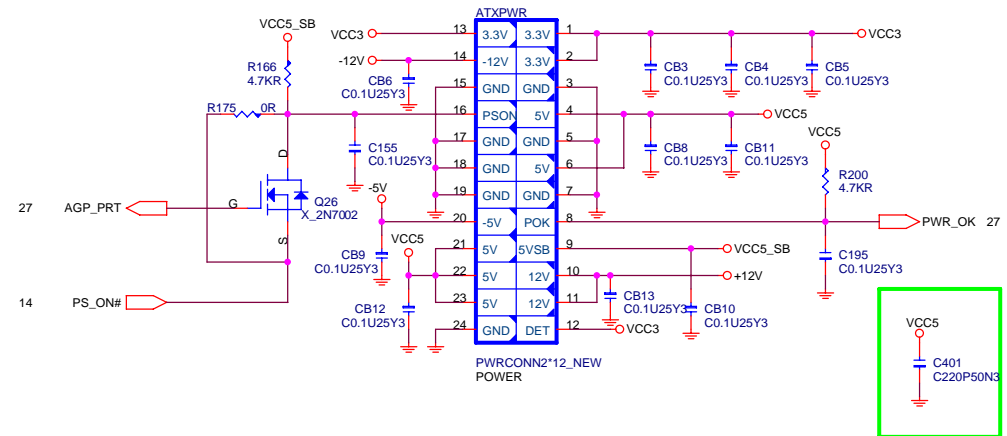
## Front Panel



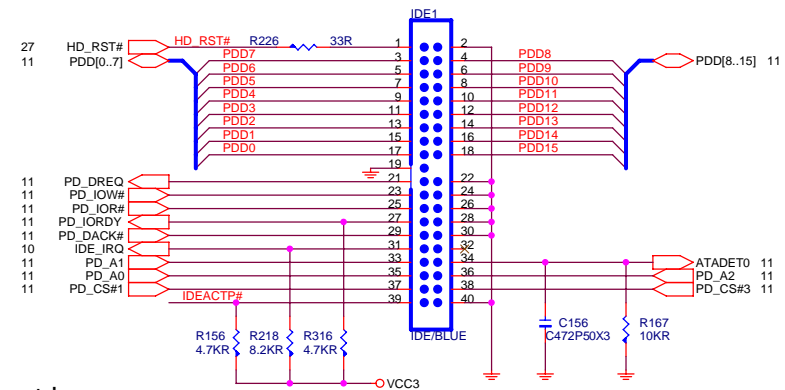
**BUZZER**



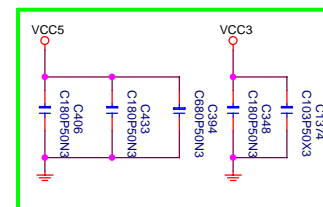
## ATX CONNECTOR



## PRIMARY IDE BLOCK



### EMI Suggestion



**MICRO-STAR INT'L CO., LTD.**

Title
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### ATX, IDE Connector & F\_Panel

Size

Document Number
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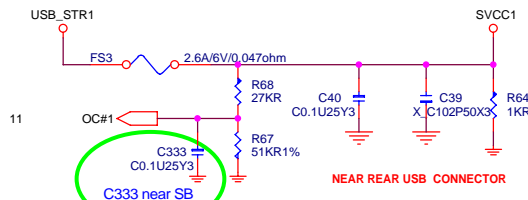
MS-7175

Rev
1.0

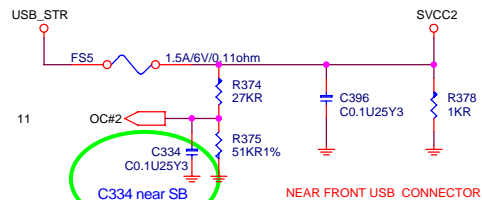
Date: Monday, August 01, 2005

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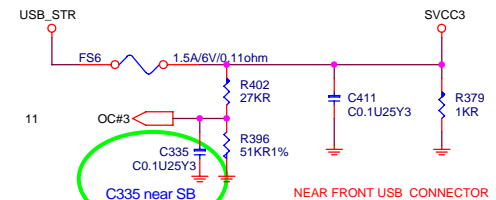
### POWER CIRCUIT FOR USB PORT 0,1,2,3



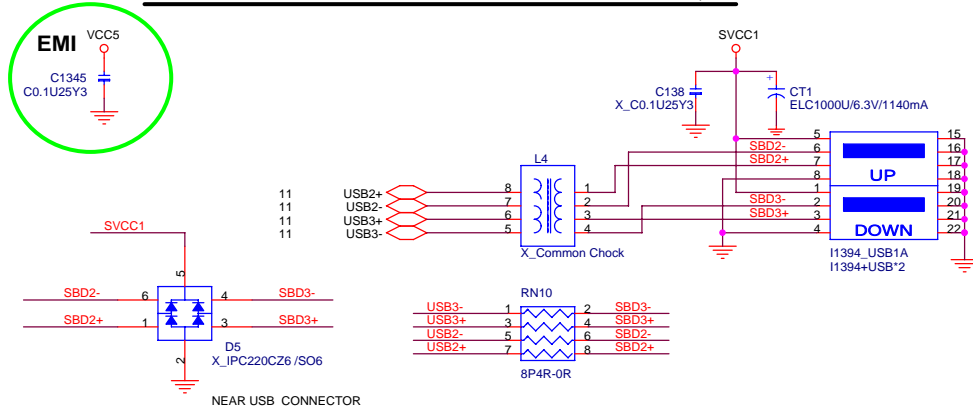
### POWER CIRCUIT FOR USB PORT 4,5



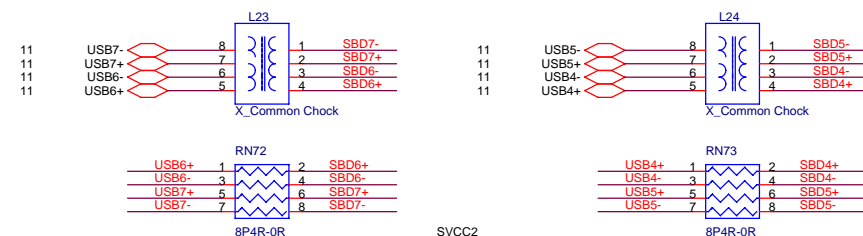
### POWER CIRCUIT FOR USB PORT 6,7



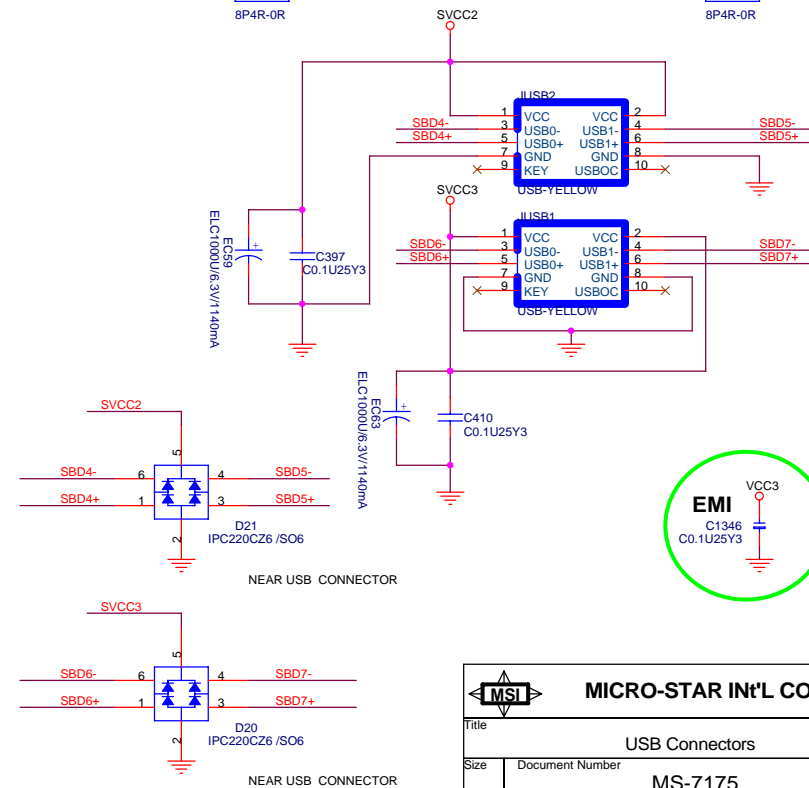
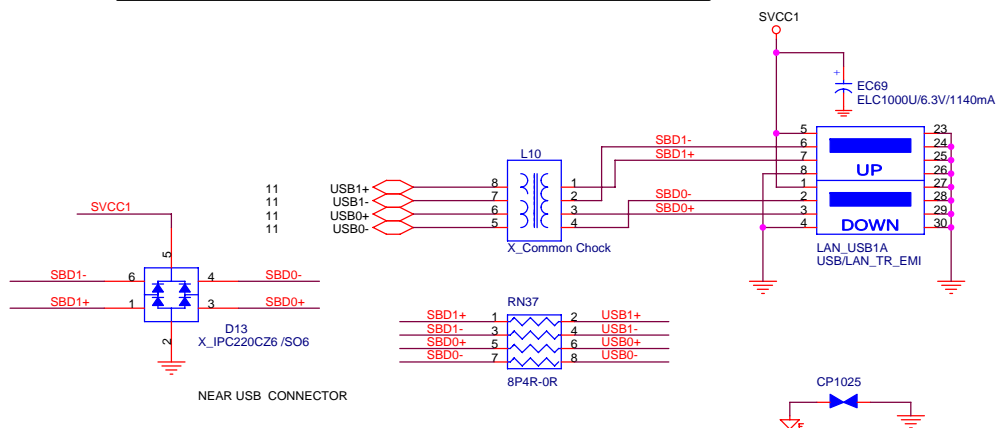
### REAR PANEL USB CONNECTOR FOR USB PORT 0,1



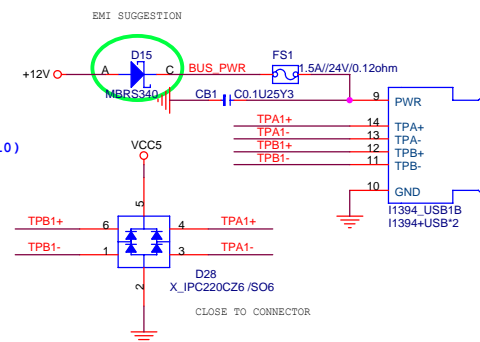
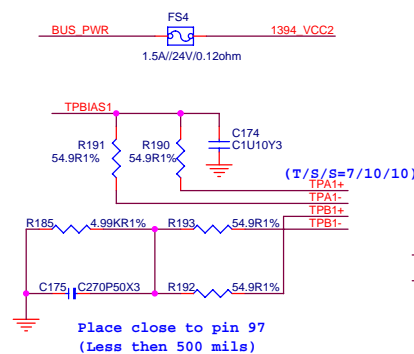
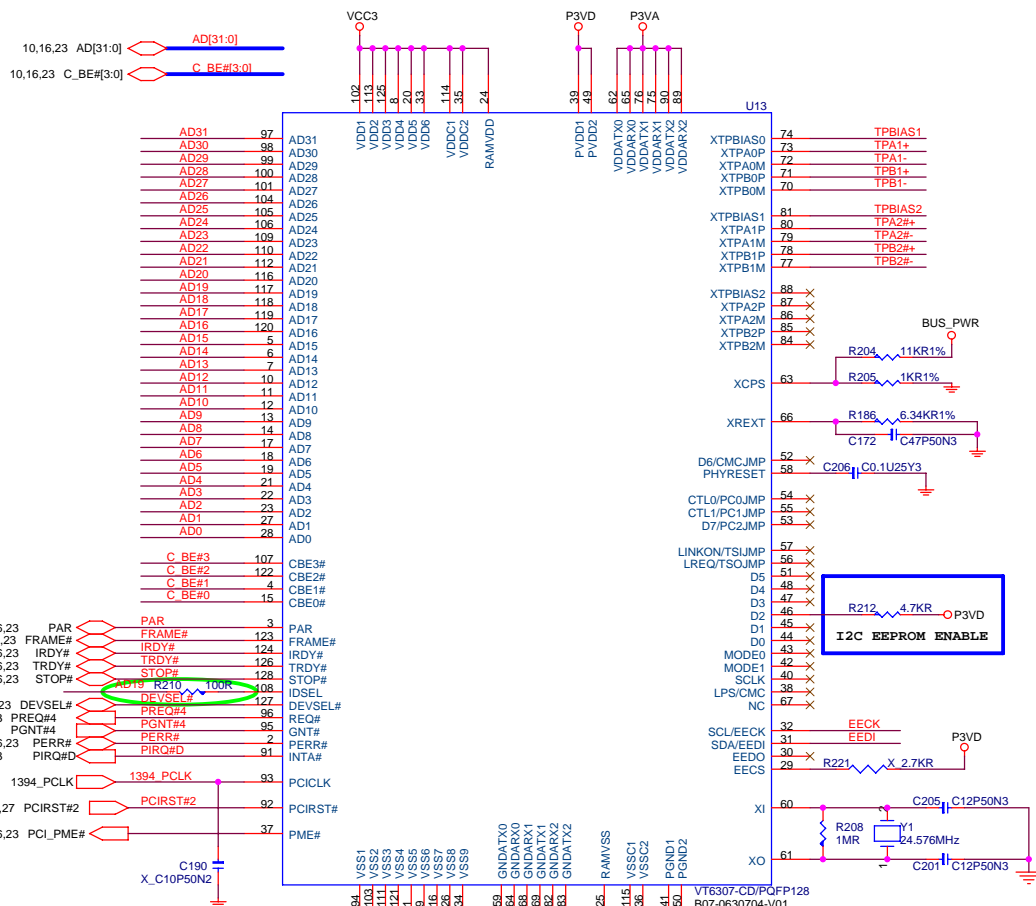
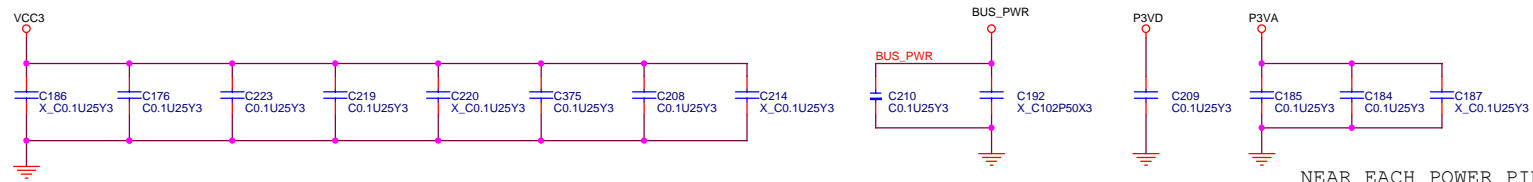
### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



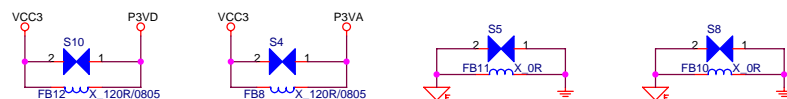
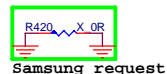
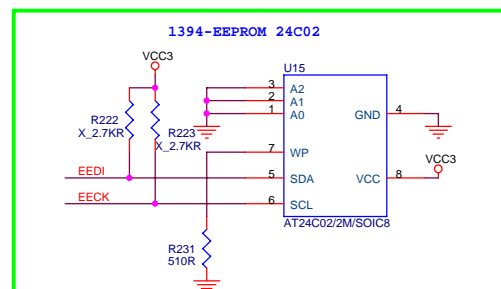
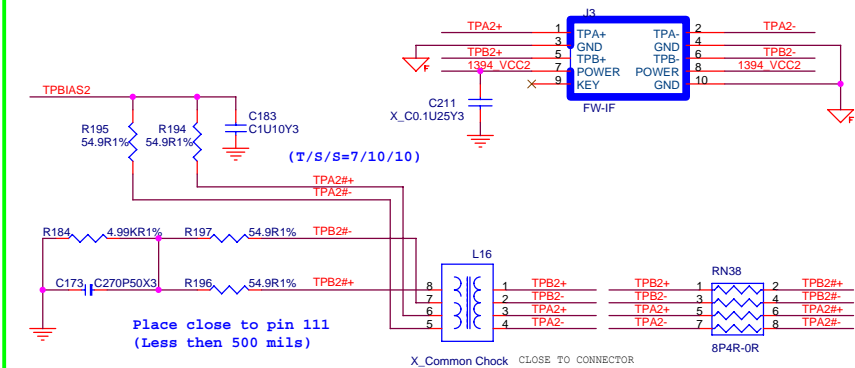
### REAR PANEL USB CONNECTOR FOR USB PORT 2,3

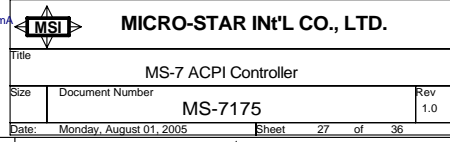


**IEEE-1394**



FRONT 1394 PORT 1





ICH6

GPIO Pin	Type	Function
GPIO 0	I	REQ6# (multifunction pin)
GPIO 1	I	REQ5# (multifunction pin)
GPIO 2	I	PCI_IRQ#E (multifunction pin)
GPIO 3	I	PCI_IRQ#F (multifunction pin)
GPIO 4	I	PCI_IRQ#G (multifunction pin)
GPIO 5	I	PCI_IRQ#H (multifunction pin)
GPIO 6	I	-RISER1 (multifunction pin)
GPIO 7	I	SIO_SMI# (multifunction pin)
GPIO 8	I	SIO_PME# (multifunction pin)
GPIO 9	I	OC#2 (multifunction pin)
GPIO 10	I	OC#2 (multifunction pin)
GPIO 11	I	SMB_ALERT#
GPIO 12	I	ATADET0
GPIO 13	I	-RISER2
GPIO 14	I	OC#3 (multifunction pin)
GPIO 15	I	OC#3 (multifunction pin)
GPIO 16	O	GNT6# (multifunction pin)
GPIO 17	O	GNT5# (multifunction pin)
GPIO 18	O	FRONT_IO
GPIO 19	O	BIOS_WP#
GPIO 20	O	Unused (multifunction pin)
GPIO 21	O	Unused (multifunction pin)
GPIO 22	OD	Unused (multifunction pin)
GPIO 23	O	Unused (multifunction pin)
GPIO 24	I/O	LAN_DISABLE#
GPIO 25	I/O	CTRL_GPI25
GPIO 27	I/O	Unused (multifunction pin)
GPIO 28	I/O	Unused (multifunction pin)
GPIO 32	I/O	Unused (multifunction pin)
GPIO 33	I/O	Unused (multifunction pin)
GPIO 34	I/O	Unused (multifunction pin)
GPIO 40	I	PREQ#4 (multifuntion pin)
GPIO 41	I	Unused (multifunction pin)
GPIO 48	O	PGNT#4 (multifuntion pin)
GPIO 49	OD	CPU_GD (multifunction pin)

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQA PIRQB PIRQC PIRQD	PCI_REQ#0 PCI_GNT#0	AD16	PCI_CLK1
PCI Slot 2	PIRQB PIRQC PIRQD PIRQA	PCI_REQ#1 PCI_GNT#1	AD17	PCI_CLK0
PCI Slot 3	PIRQC PIRQD PIRQA PIRQB	PCI_REQ#2 PCI_GNT#2	AD18	PCI_CLK2
LAN	PIRQC	PCI_REQ#6 PCI_GNT#6	AD22	LAN_PCLK
1394	PIRQD	PCI_REQ#4 PCI_GNT#4	AD20	1394_PCLK

SIO

PIN NAME	USAGE	Input/Output	NOTES
GPIO34	IRR <sub>X</sub> (multifunction pin)	OUTPUT	
GPIO35		INPUT	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1		P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM 2		P_DDR3_A/N_DDR3_A P_DDR4_A/N_DDR4_A P_DDR5_A/N_DDR5_A
DIMM 3		P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B
DIMM 4		P_DDR3_B/N_DDR3_B P_DDR4_B/N_DDR4_B P_DDR5_B/N_DDR5_B

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI 1-3, PCI_E X 16, LAN
PCIRST#2	SIO,1394,LPC debug port,FWH
PCIRST_ICH6#	MS7
HDDRST#	Primary IDE

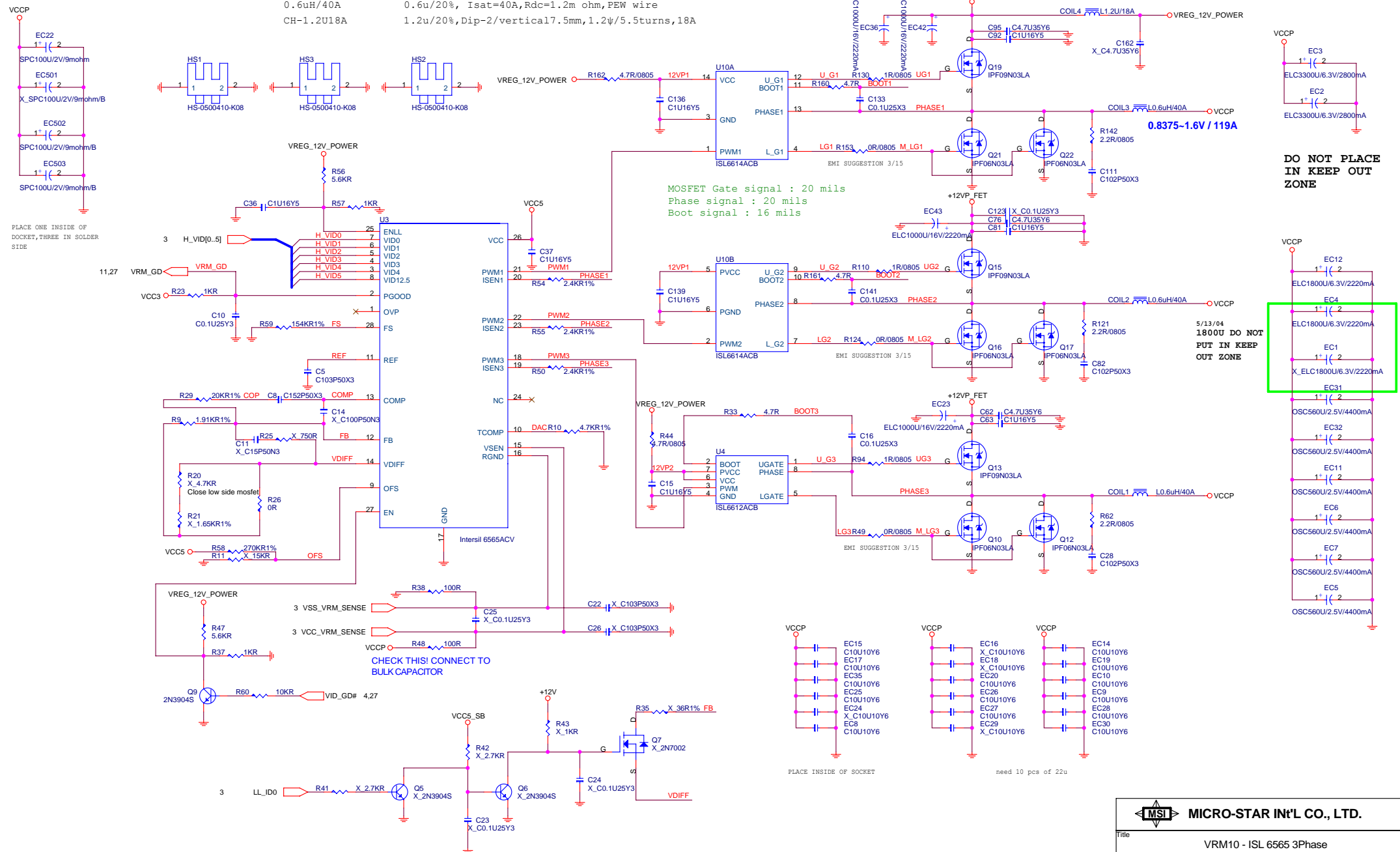
JUMPER SETTING

<b>JBAT1</b>	(1-2) NORMAL	(2-3) CLEAR

## Voltage Regular Module


IPF06N03LA  
C100U2SP  
.CD3300U6.3EL25  
560u\_2.5V  
1800UF/6.3V  
0.6uH/40A  
CH-1.2U18A

Rds(on)=8.7mΩ(@4.5V, 30A), Vgs(on)=1.2~2V, Id=50A, Ciss=3110pf, Qg=10nC, Vds=25V, Vgs=±20V  
ESR<13mΩ, Ripple cur.<2.7A, Lc<12uA, 105C  
ESR=12mΩ, Ripplecur.<2800mA, 105C, longlife3000hrs, KZGSeries  
ESR=6mΩ, Ripplecur.=4400mA, Lc.<500uA, 105C/2000hrs  
ESR<12mΩ, Ripplecur.<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ series  
0.6u/20%, Isat=40A, Rdc=1.2m ohm, PEW wire  
1.2u/20%, Dip-2/vertical17.5mm, 1.2u/5.5turns, 18A



DO NOT PLACE  
IN KEEP OUT  
ZONE

5/13/04  
1800U DO NOT  
PUT IN KEEP  
OUT ZONE

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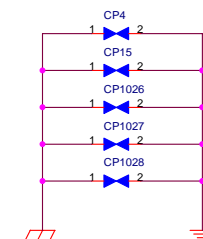
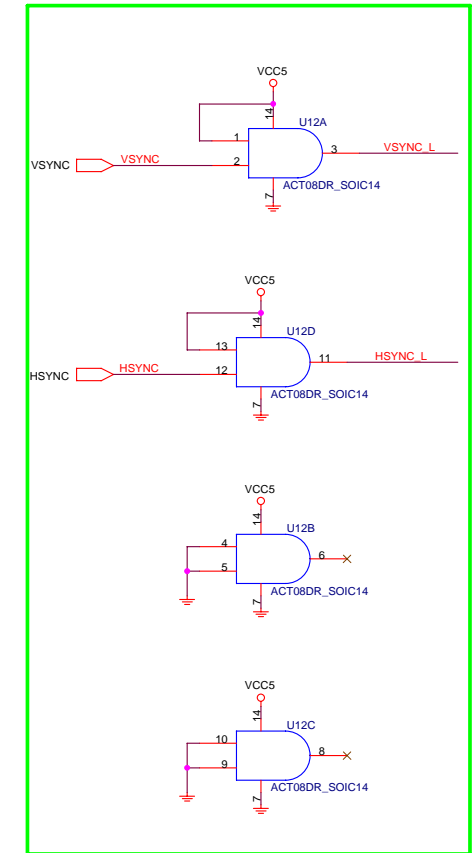
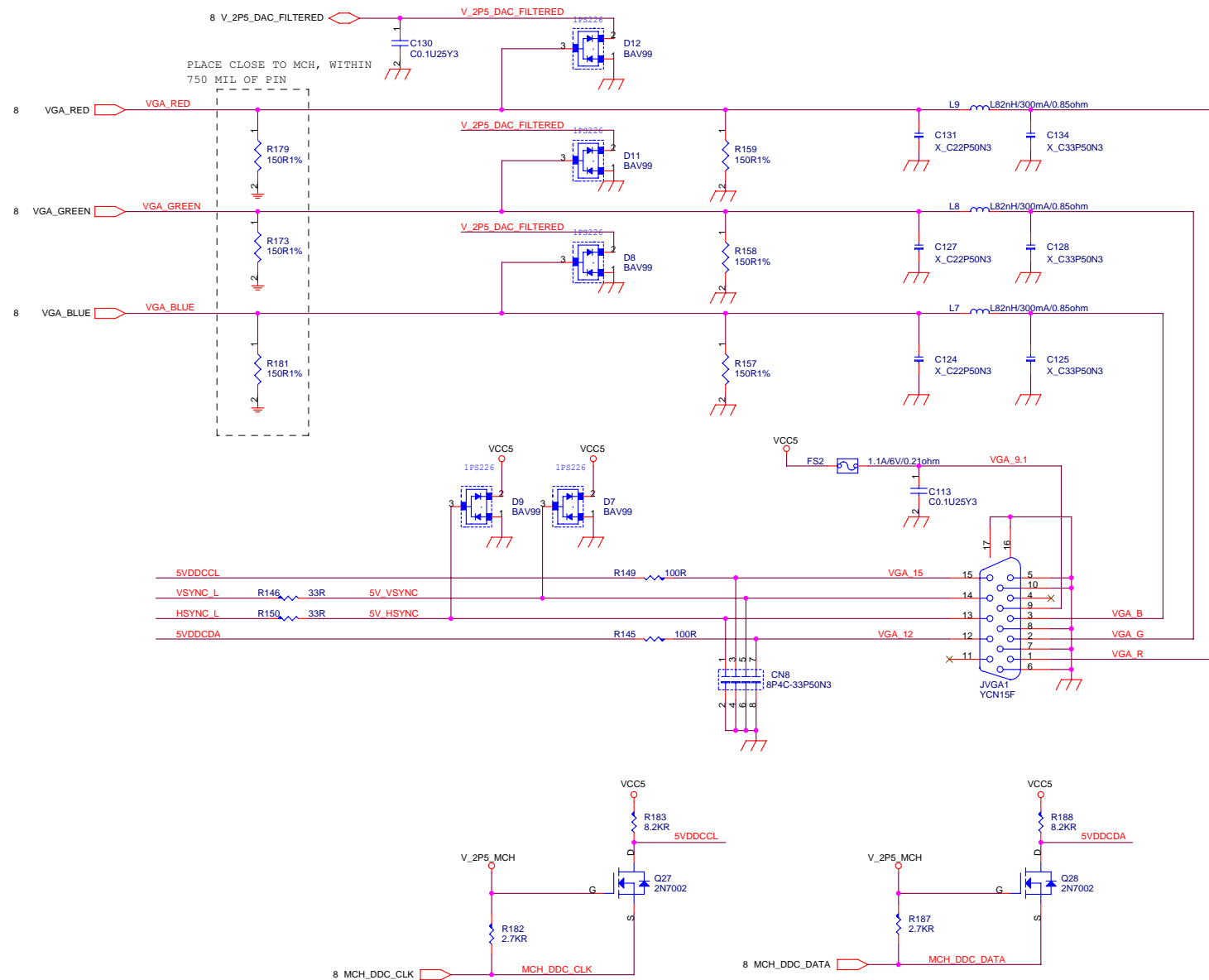
Title	VRM10 - ISL 6565 3Phase
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# Video Connector



## EMI Modify:

- 1.Add VCC5's 104P(C1360,C1361)near RN16 and C2...page14
- 2.Change to VCC5's 180P(C406,C433); VCC5's 680P(C394)...page24
- 3.Change C348 to VCC3's 180P; add VCC3's 103P(C1374) near C263...page24
- 4.Add VCC\_DDR's 101P(C1353,C1354,C1355,C1356)near MH5 and R220...page17&21
- 5.RN57,RN58 change to single 0402 resistor(R427,428,429,430)...page13
- 6.Reserve 10P(C1357,C1358) in U17.B13 and U17.B14...page16
- 7.Change Lan connector PN from N58-22F0061-S42 to N58-22F0061-F02...page17
- 8.Reserve 10P(C1359)in LAN\_PCLK(page16)
- 9.Add VCC5's 180P(C1365,C1366) to replce the EC60...page27
- 10.Add VCC5's 180P(C1362,C1364) and 56P(C1363) to replce the EC58...page27
- 11.Add 102P(C1368) in SUS\_LED...page24
- 12.Add 101P/0402(C1370) in FRONT\_IO#...page18
- 13.U11\_X2's X1/X2; U21's XX1/2/3/4 to GND...page10&17
- 14.MH4 share to GNDF and GND...page17
- 15.Add VCC3's 104P(C1367) near Q24...page27
- 16.Add VCC5's 104P(C1369)near C132...page22
- 17.Add VCC3's 220P/0402(C1371) near LAN\_PCLK's via...page16
- 18.Add VCC3\_SB's 103P(C1372,C1373) near R299,R382...page11&27
- 19.Change CB46 to VCC3\_SB's 103P...page12
- 20.Change R344 to VCC3's 104P...page10

## Samsung Request:

- 1.Stuff R18 and no stuff R16 for 2E/4E request(page14)
- 2.Assign 2 GPIO to add JCOM1/FDD detection(page14)
- 3.Reserve standby LED to indicate the G3->S5 state(page27)
- 4.FRONT\_IO# connect to GPIO of ICH6(page11)
- 5.Reserve R431=10Kohm pull down resister(page15)
- 6.Add protect ckt for winbond I/O PSIN failure issue(page24)
- 7.Add audio jack sensing pin to front audio connector(page18)
- 8.No stuff for CD\_IN1(page18)

- 21.Change C403 to 180P and C401 to 220P...page23&24
- 22.Add 103P in C278, C279...page17
- 23.Stuff C149=0.1uF(100nF),C159=10pF...page17
- 24.Change C1345 to 104P...page25
- 25.Connect I/O GND and GND in LAN connector
- 26.Change C181 to 680P, C358 to 103P and C120 to 102P
- 27.Add 103P(C1375,C1376,C1377) in SB bottom side...page12
- 28.Add 10nF in ACTLED#/1000LED# near connector side(C143,C157)...page17

5/19  
updated

## MSI HW Modify:

- 1.Change R301,R302 from 10Kohm to 2.2Kohm can pass the rising/falling time of SMBus(page11)
- 2.R284 change to 15ohm and remove the C309,C315 can improve the LPC signal quality(page27)
- 3.RN64 change to 33ohm can improve the audio signal quality(page11)
- 4.L7,L8,L9 change to inductor and remove the C134,C128,C125 can pass the RGB signal rising/falling time spec(page30)
- 5.Exchange the EE\_DIN1 and EE\_DOUT1 for circuit error(page16)
- 6.Add protect circuit for winbond I/O PSIN failure issue(page24)
- 7.Remove the C149,C159 can pass LAN quality issue(page17)
- 8.Change R50,R54,R55 from 5.1Kohm1% to 2.4Kohm1% for OCP adjustment(page29)
- 9.Change R9 from 3.9Kohm1% to 1.69Kohm1% for droop adjustment(page29)
- 10.Change C8 from 5600pF to 1500pF/X7R and remove C14 for compensation adjustment(page29)
- 11.R58 stuff 210Kohm1% for offset adjustment(page29)
- 12.EC65,EC66 stuff the SP cap(100U/9m ohm) for pass the loadline spec(page29)
- 13.Change EC11,EC5,EC6,EC7 to OSCON cap (560U/2.5V) for pass the loadline spec(page29)
- 14.CN4,CN5,CN6,CN7 and C103 change to 180P for winbond suggestion about PRT test(page 14)
- 15.RN24,RN16,RN13,RN18 and R141 change to 22ohm for winbond suggestion about PRT test(page14)
- 16.CN1 change to single capX4(page14)
- 17.Reserve EC69 for rear LAN\_USB port's power(page25)

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Samsung Request:

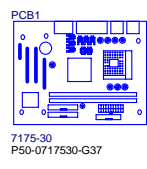
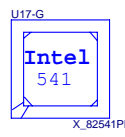
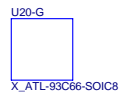
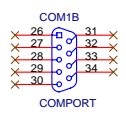
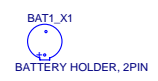
- 1.Reserve the GPIO 28 pin of ICH6 for 82541PI controller disable function(page11)
- 2.Reserve 0ohm pad(R442) for depress the FRONT\_IO# noise(page18)
- 3.Add dual LED for HDD active and into suspend state indication circuit(page24)


MSI HW Modify:

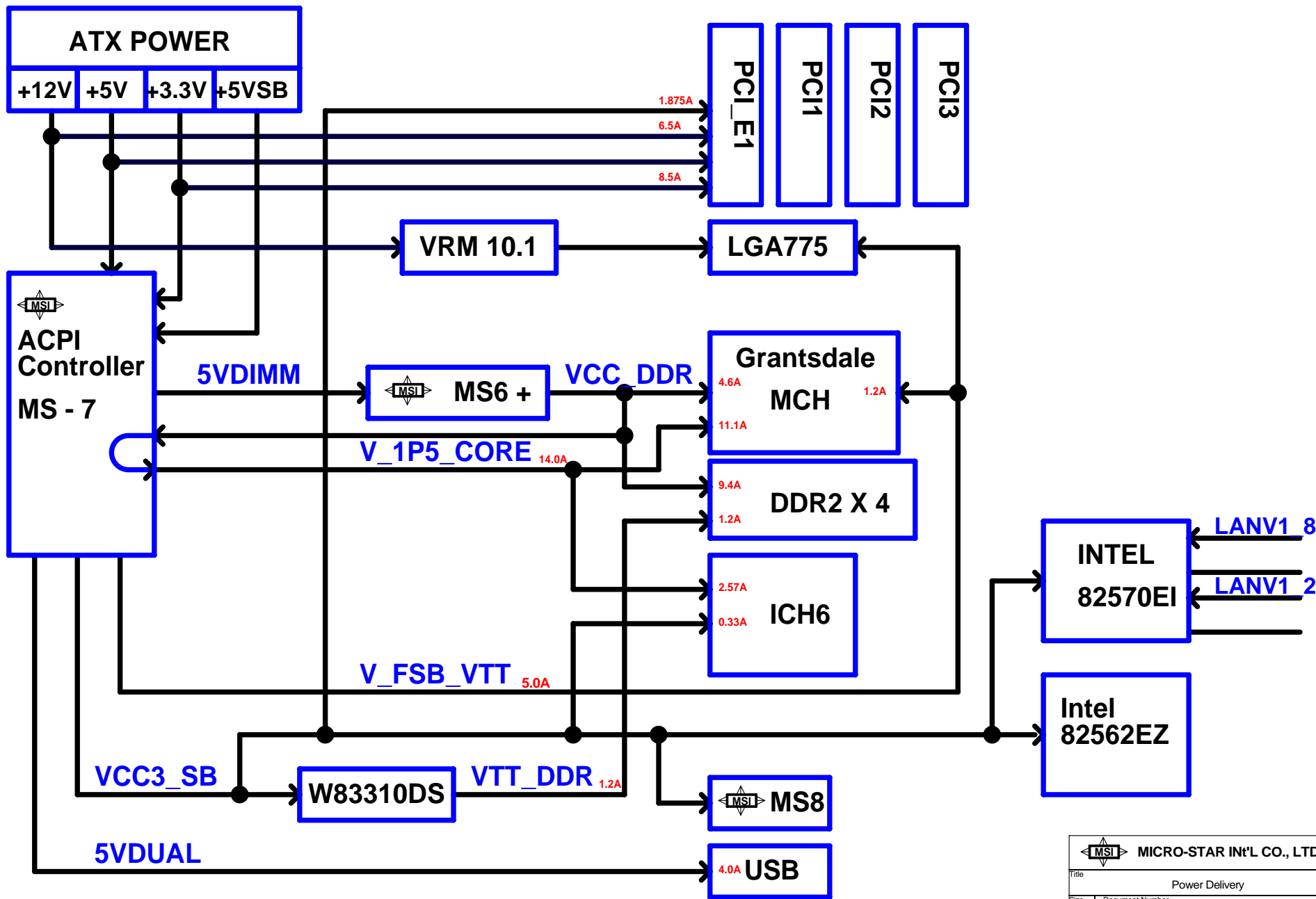
- 1.Exchange the EE\_DIN1 and EE\_DOUT1 for circuit error(page16)
- 2.Remove the JIR1(page14)

EMI Modify:

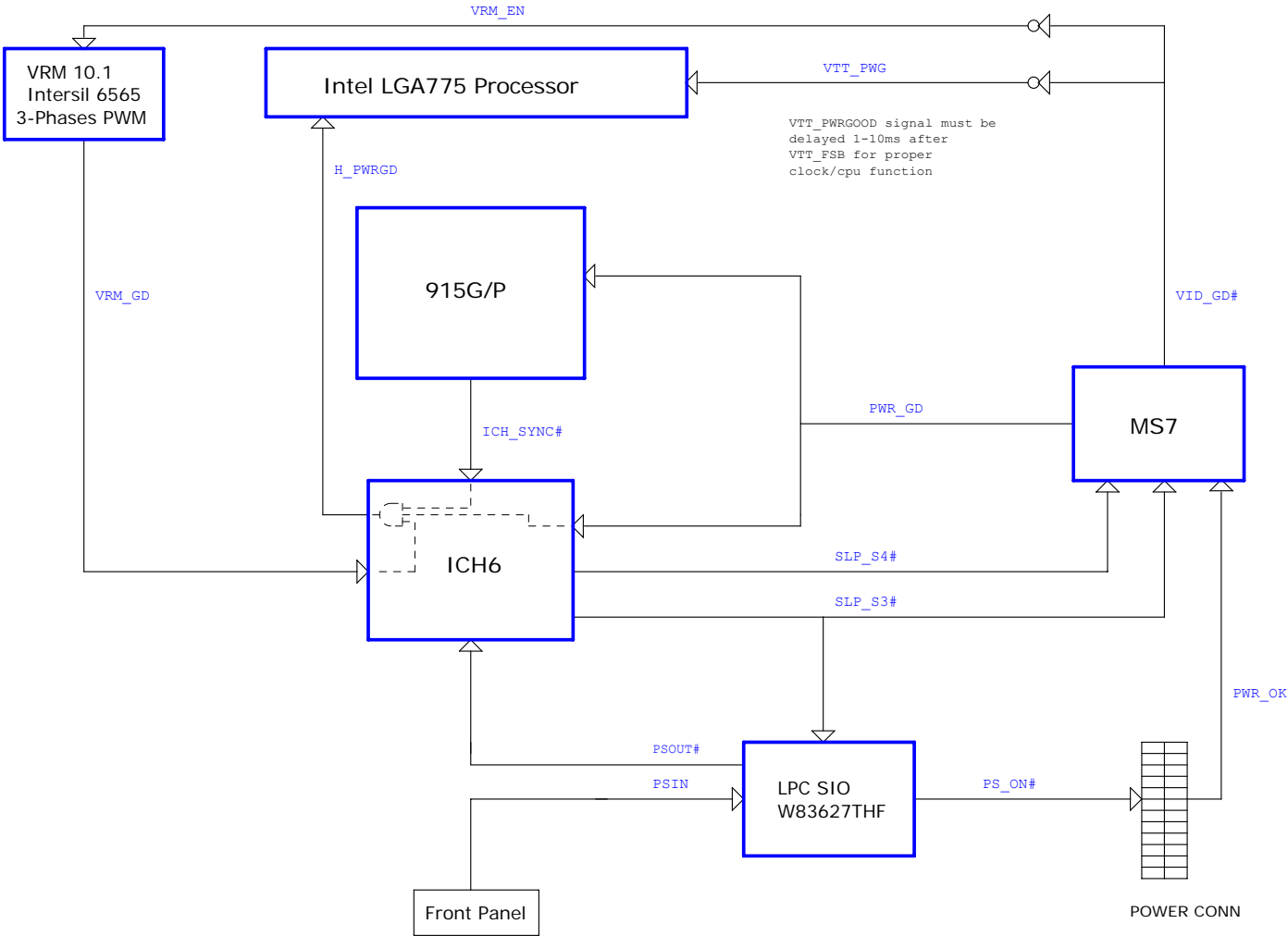
- 1.Add VCC3\_SB's 102P=1nF(C1388,C1389) and V\_1P5\_CORE's 102P=1nF(C1387) in ICH6 bottom side(page14)
- 2.Change C359 from 10pF to 33pF(page11); Remove the C409(page18); Stuff the CB48 to 100nF(page10)
- 3.Stuff the C1364 to 1nf(page27); Remove the C1362, C1363(page27)
- 4.Add filter(0.1uF) in JCOM1\_5(page14)....ps:Stuff the R409=0.1uF
- 5.Stuff the C365 to 1nf and move C407 to the nearby JP\_F1(page24)
- 6.Stuff the CB14 and CB18 to 0.1uF(page16, 17)
- 7.Add VCCL1.8's 0.1uF(C1384)near the LAN connector(page17)
- 8.Change RN40 and RN42 from 0ohm to 33ohm(page16)
- 9.Add X2\_KINN\_CTRL\_15/12's 0.1uF X2(C1385, C1386)....page16
- 10.Reserve the protection diode(D28) near rear 1394 port(page26)
- 11.Stuff the C1346, C1366 to 0.1uF and change C1365 to 0.1uF(page25, 27)



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PWROK MAP



RESET MAP

